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Goddard Space Flight Center

National Aeronautics and Space Administration

A STUDY TO DETERMINE THE THERMAL CHARACTERISTICS OF COTS BOARDS AND THEIR BEHAVIOR IN A VACUUM

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SUMMARY

A study has been conducted to determine the thermal characteristics of three commercial-off-the-shelf electronic (COTS) circuit boards; and temperatures have been predicted for the boards when they are operated in vacuum conditions. The COTS boards used for this study are those in the WinSystems PC104 computer/controller. The primary thermal characteristic of interest is the chip power dissipation. The confidence level/accuracy associated with the chip power dissipation determination has been evaluated by comparing calculated temperature results for the operating boards against measured temperatures and measured power dissipation. The measured data came from tests in which the boards were operated in a room ambient environment while running the Norton Utilities software. During the tests, the boards rejected heat to the room via natural convection or forced convection heat transfer (in addition to the always present radiation heat transfer). Three air speeds were used for the forced convection tests. Chip heat dissipations and temperatures were calculated with SINDA85 models representing each board as it operated in each of the convective heat rejection situations.

A high level of confidence can be associated with the circuit board thermal characteristics derived from this study. The high confidence level derives from the less than 4 degrees centigrade of correlation (difference) between measured and calculated temperatures for almost all of the chip/board areas considered. The typical correlation was less than 2 degrees centigrade. Calculated total power dissipation was approximately 3.20 watts versus the 3.76 watts measured. The error in the calculated power might lead to a maximum error in temperature prediction of about 4 degrees centigrade.

The temperature predictions indicate that the boards will be able to operate in a vacuum with a maximum sink temperature of 21 degrees centigrade, assuming that the chips can tolerate a reasonable (although unconfirmed) maximum case temperature of 70 degrees centigrade.

INTRODUCTION

The use of commercial-off-the shelf (COTS) electronic circuit boards in certain space-borne equipment may represent an effective and economical alternative to using the typical space qualified electronics. Most of the current space qualified electronics have been designed and built in small quantities, their costs not benefiting from the economies of large scale production that are characteristic of COTS boards manufacture.

As with boards designed specifically for space applications, testing would be required to verify the viability of COTS boards in a space application. Included in the verification process would be a thermal test. Unlike mechanical tests which can be performed in room-like conditions and yield results indicative of the performance of the board in space, a thermal test done in a room ambient environment would not result in flight-like temperatures because of the increased heat transfer produced by convection currents. On the other hand, performing a thermal test of a COTS board under more flight-like, vacuum conditions presents two problems: the first is that thermal vacuum tests are costly, the second is that components on the board may be destroyed by overheating prior to obtaining any useful information from the test.

Hence, thermal testing of COTS boards must be non-destructive, done in a manner which elucidates their thermal characteristics, and done as cheaply as possible. In fact, the thermal test would be part of a larger analytical effort. The effort described in this document, and proposed as a means for future COTS board evaluation, involves the gathering of temperature data on COTS boards operating in a convective heat transfer environment, followed by the mathematical analysis of that data to determine the board's thermal characteristics. Specifically, the thermal test(s) provide measured temperature data which are used to correlate (adjust) a thermal math model so that it accurately represents the test scenario. The correlated model yields power dissipation information for particular components (chips). This power dissipation information can then be used in a thermal math model of the flight scenario to predict flight temperatures. Furthermore, the thermal math model would aid in determining any board modification(s) needed to control or reduce flight temperature predictions. Therefore, the thermal test itself, when done in convective conditions is used mainly to compensate for the lack of readily available (common to the COTS world)

component power dissipation information. If such information were available, the thermal test would not be absolutely necessary, although the analysis and predictions of flight temperatures would be. Related guideline and procedural documentation is listed in the references.

The three circuit boards used in the present analysis are those that comprise a WinSystems PC104 computer. The boards are designated as follows:

- Processor
- Input/Output (I/O)
- VGA

Computer and individual circuit board dimensions are contained in Appendix A. The selection of these circuit boards was not based on any intention to use them in a spacecraft, rather they were chosen mainly because of their availability and similarity in computational performance to existing flight hardware.

Both natural and forced convection (in addition to radiation) conditions were used to gather thermocouple measurements (temperature data) for each of the three boards. In addition, IR temperature measurements were made of each board using an infra-red sensitive camera in one of the natural convection conditions. The boards ran the Norton Utilities Intel 80386 compatible program in a DOS environment during the thermal test. This software ensures rather intensive use of all board components; thus guaranteeing high chip power dissipations.

METHODOLOGY

Testing

In order to quickly determine which chips dissipated the most power, each of the three boards was first subjected to an IR camera examination. The IR images gave a good indication as to the location of all of the relative maximum temperatures – information critical to the modelling effort since chips at those locations are the major heat producers and drive the general board temperature distribution. IR temperature measurements of the board were corrected to account for a non-realistic board emittance of 0.75 used in the camera setting. Although not measured for this effort, a more realistic overall board emittance of 0.85 was measured in the testing described in Reference 1, and used to correct the IR camera measured temperatures. The corrected IR camera temperatures are shown in Appendix B. The normal arrangement for PC104 boards is a stacked configuration. For the IR imaging, the stacked arrangement was maintained, but the stack was rotated so that the boards were vertical. Because of the stacking, only one board at a time could be imaged. The position of the boards was interchanged to bring each of the boards to the forefront for imaging. The IR imaging was done in a room at approximately 21 degrees centigrade; and, the boards were shielded from any currents produced by the room ventilation system. The chips were running the Norton Utilities Intel 80386 compatible program in a DOS environment during the test.

After the IR imaging, type T, 32 guage thermocouples were attached to the top surfaces of the chips. The thermocouples were attached with aluminum tape. The aluminum tape was covered with 0.004 inch thick Kapton tape to re-establish the high emittance of the top surface of the chip. The boards were then delivered to the University of Maryland's Glenn L. Martin (GLM) wind tunnel facility where, in addition to operating boards under natural convection (Vair = 0) conditions, a fan/plenum/diffuser device was used to deliver a flow of air at a known speed to each of the three operating boards in its turn. The boards were arranged as shown in Figure 1, downstream of a conical diffuser which produced a uniform flow field. Concern over boundary layer separation from the upstream edge of the top surface of the upper board prompted the use of a hemicylindrical attachment to the upstream side of the board stack. This "streamliner", also shown in Figure 1, was attached to the stack with tape.

Each of the three boards (operating) was tested at the top of the stack by exposing it to the air flow. Only the upper surface of the board at the top of the stack was of particular interest in this test/analysis. Modeling the stack as a whole would have greatly complicated (and increased the error in) the analysis by

having to account for the developing flow in what is essentially a duct formed by the top and middle boards. So, it was thought that to reduce the analysis error, it was imperative to restrict air flow to the upper surface of the top board (and, consequently, the modeling of heat transfer to that surface). Air flow under the top board (and through the stack) was prevented by wrapping duct tape around the stack. The duct tape enclosure, though, could have promoted natural convection heat transfer between the middle and top boards which would have complicated the analysis and defeated the purpose of the tape. Hand calculations, however, indicated that natural convection between the middle and top boards was not a factor, and that heat transfer between the two boards would be limited to conduction (simple enough to include in the model). Hand calculations also indicated that heat rejection from the middle board in the stack to the duct tape surfaces and the lower board (and not the top board) might be sufficient to prevent overheating of the middle board. Interestingly, the test results indicated that while the use of duct tape did not complicate the analysis, it was not necessary either. Two tests were done at the Vair = 7.07 m/s with and without the streamliner and the downstream piece of duct tape to determine the effect of air flow under the top board. Since the average board temperature (for the top board, with the streamliner) was within 2 degrees centigrade of the free stream air flow temperature, subjecting the bottom surface (as well as the top) of the board to forced convection had less than a degree centigrade effect on chip temperatures (see the results in Appendix C). A photograph of the test set-up, including the duct tape, at the GLM facility is shown in Figure 2.

Board and air temperatures were measured at four airspeeds for each board: Vair = 0 (i.e. natural convection), 4.17 , 7.07, 15.0 meters per second. A thermocouple data logger system was used to monitor the temperature at 32 locations continuously and record them every 30 seconds. Steady state temperatures were also manually recorded. The manually recorded temperatures are contained in Appendix C. The thermocouple numbering system corresponds to that shown in Appendix B. Temperature measurements were made of various chips. Measurements were also made at three places on the boards: one TC was used under the hottest component, another two were located at disparate locations on the board. The board temperature was measured as a means of assessing the rate of conductive heat transfer between boards in the stack.

Analysis

Chips associated with relative maximum temperatures were treated as heater nodes in a SINDA85 model of the board. A model of each board was made with the conductive effect of the embedded copper planes included (see Appendix D). The model calculates the board and chip local convective heat transfer coefficient as a function of downstream position. These board models were used to deduce the power dissipation of the chips by correlating to the forced convection scenarios. Then, by using those chip power values, temperature predictions for the natural convection scenarios were made. The natural convection scenarios are comprised of:

- one horizontal orientation for each board (i.e. Vair = 0, done at GLM facility)
- one vertical orientation for each board (i.e. the IR camera imaging of each board)

The temperature predictions for the natural convection scenarios were then compared to measured values in order to evaluate the accuracy of COTS board thermal analysis. Having proven the analysis sufficiently accurate, the final step was to predict temperatures for each board operating in an exclusively radiative heat transfer environment.

Appendix E contains the nodal diagrams used to model the boards. Appendix E also contains, as an example, the SINDA85 model (CONV3.INP) used to calculate temperatures for the forced convection situations. The natural convection and vacuum temperature calculation models (not in the Appendix) are named NCONV2.INP and RAD.INP, respectively.

Nodal size is 0.236 inches square and there are 240 nodes per board not including chip nodes. Each of the major dissipating chips were assigned nodes. The numbering convention for them simply uses the number of the underlying board node prefixed with a "9". The chips varied in size from 2 nodes to 25 nodes.

Only the high dissipating chips were modeled. Given the low heat dissipation of most chips and the fact that the sum of pin and air conduction was at least two times (much higher in natural convection cases and for surface mount chips) the convective conductance associated with the top of the chip, the temperature difference between these low dissipators and the underlying board nodes is negligible.

The chip nodes were connected to the board with conductors representing pins or air or both (such as along the edge of the chip). Pin conduction was calculated as 0.0016 W/deg. C per edge node for surface mount chips, 0.0033 W/deg. C per edge node for plug-in chips. Air conduction was calculated as 0.0051 W/deg. C for surface mount chips; air conduction was negligible for plug-in chips. Radiation conductors were connected to all nodes with the emittance of all surfaces, including chips, taken as 0.85. The area of the room's walls was considered to be infinite.

Convection heat transfer is strongly influenced by the size of the boundary layer. In the test set-up, the boundary layer began its development at one edge of the board (the leading edge) and grew larger as the flow progressed to the downstream edge (trailing edge) of the board. The corresponding variation in the heat transfer coefficient, "h", (from the leading to the trailing edge of a board) was rather large: a ratio of approximately 3.5 to 1. This variation was valid for both vertical natural and forced convection (and regardless of the airspeed). Prior to starting the modeling, therefore, there was a concern that such a large variation in "h" over a relatively short distance (approximately 3.6 inches) might introduce a rather large error. A few cases in point:

- for Vair = 7 m/s, h=44.9 $W/m^2/deg.$ C @ x=0.5 inches
  h=18.4 $W/m^2/deg.$ C @ x=3.0 inches

- for Vair = 15 m/s, h=65.7 $W/m^2/deg.$ C @ x=0.5 inches
  h=26.9 $W/m^2/deg.$ C @ x=3.0 inches

where 'x' is the distance from the upstream (leading) edge of the board.

The results (discussed below), however, would indicate that the impact of this and other errors was very limited. The model incorporates an algorithm which calculates the Nusselt number 'Nu' as a function of the downstream position of a given node and the Reynolds or Grashof (in the natural convection cases) number of the air at the given node; excepting the horizontal natural convection cases, where an average "Nu" was used. In all cases, the non-dimensional numbers indicated laminar flow. Another algorithm calculates the heat transfer coefficient 'h' from the Nusselt number, the relationship being :

$$h = Nu*k/x$$

where k = thermal conductivity of air at film temperature
x = distance from leading edge of board or effective length "L'" (see below) in the case of horizontal natural convection.

The following Nusselt number formulae were used:

- for forced convection, $Nu_x = 0.3925(Pr^{1/3}Re_x^{1/2})$, based on the average of the formulae for constant temperature and constant flux boundary conditions.

- for horizontal natural convection, $Nu = 0.60(Gr_L \cdot Pr)^{0.25}$ where L' = 1/(1/(stack height)+1/(stack width)). The natural convection occurring on the top surface of the stack was driven by heat transfer over all surfaces of the stack, therefore, the characteristic dimension that was used for the 'Nu' and 'h' calculation is "L'" rather than the length or width of a circuit board.

- for vertical natural convection, $Nu_y = 0.59(Gr_yPr)^{0.25}$, based on natural convection heat transfer from a vertical plate..

RESULTS & DISCUSSION

Figures 3, 4, & 5 are the IR images of the vertically oriented PC104 boards. The brightest (and hottest) chips in those images are located at relative maxima in the temperature distribution; and, therefore, they are the primary determinants of the temperatures of all other areas/chips on the board. The hottest chips, being the major heat dissipators, are the ones that were treated as heater nodes (a form of boundary node which enables easy calculation of net heat leaving the node) in the thermal math models. Most of these chips were treated as constant temperature surfaces even though a gradient was apparent in the IR image. During the testing at GLM lab, large pieces (covering practically the entire chip) of 0.004 inch thick aluminum tape were attached to the top surfaces of the chips. The tape eliminated or reduced most intra–chip (lateral) gradients to negligible levels. But, as the IR image of the VGA chip shows, it possesses a particularly strong temperature gradient. Although moderated, the gradient remaining after tape application was calculated and accounted for in the modeling.

The chip temperatures seen during the forced convection tests were imposed on the heater nodes in the thermal math models, and forced convection and radiation boundary conditions (using a board emittance = 0.85) were established for all board and chip nodes in the model. The chip power dissipations thus derived are shown in Table 1.

The total power dissipated by all three boards was measured at 3.76 watts (there was an occasional transient of +/- 0.2 watts). The 0.59 to 0.67 watt discrepancy between measured and calculated powers (3.09 to 3.17 watts) is not very great considering that only 8 of the 18 chips on the three boards were assumed to have any dissipation. If the difference in dissipation is distributed evenly amongst the 10 chips not modeled with dissipation, the resulting 0.059 watts/chip is only a slightly high estimate of the dissipation of a low dissipating chip, such as a memory chip. Furthermore, the 0.059 watt/low dissipator chip estimate would certainly be reduced if one accounted for the errors (see below) associated with the calculation of heat transfer coefficients, local velocity assumptions, temperature measurement, unaccounted heat losses, etc. Therefore, consideration of the calculated chip dissipations alone leads to a good level of confidence in the model; but, the confidence level was improved by an additional two analyses:

First, measured board and chip temperatures were compared with those calculated using the model. The comparison was made by considering chips or board areas located away from the heater nodes. As demonstrated by comparing Figures 6A and 6B, temperatures at processor board locations far from an asterisk were correlated to within 2 degrees centigrade or less of the measured temperatures. Figures 7A & 7B and 8A & 8B show similar results for the other boards. These Figures indicate that the calculated board temperature distribution is very close to the measured one; lending additional credibility to chip power dissipation results. Note that the asterisks mark hot spot/heater node temperatures and, as previously mentioned, the hot spot temperature and the heater node temperature must be the same by definition.

The second confidence building result is obtained by comparing the calculated against the measured board/chip temperature distributions for the natural convection situations. Unlike in the forced convection modeling, temperatures *were calculated for the dissipating chips* as well as other chip/board areas. Figures 9A & 9B compare the measured against the calculated temperatures of the processor board/chips in the horizontal natural convection scenario. In this scenario, the heat dissipation (calculated using the forced convection models) was impressed on the nodes representing the major heat dissipating chips in the natural convection models. Also, the roughly 0.63 watts discrepancy between calculated and measured power dissipation was accounted for by distributing 0.63 watts evenly over all board nodes. Figures 10A & 10B and 11A & 11B show the horizontal natural convection results for the other boards. In general, the correlation was good: less than 4 degrees centigrade difference between measured and calculated values. In these figures, the major dissipators (the same as those in the forced convection comparison) are marked both with an asterisk and an identifying letter used for cross reference to Table 1.

The vertical natural convection situation that existed for the IR camera testing was also correlated. While the results were not quite as good as the aforementioned correlations, they were, nevertheless, reasonable. Especially when considering that the sources of error for this correlation were more numerous; particularly

conspicuous being the error introduced by correcting for the wrong camera emittance setting. Also, the author was not a witness to the IR camera test, and no record was kept of the exact test arrangement and board configuration. Hence, small details that could influence temperature predictions (although probably a small amount) go unaccounted for. Therefore, given the lower reliability of the vertical natural convection correlation, its results have been relegated to Appendix B.

Figures 12A & 12B & 12C indicate the temperature predictions for the PC104 boards if they, hypothetically, rejected heat solely through radiation. The chips would probably survive the predicted temperatures, assuming that some of them can tolerate a case temperature approaching 70 degrees centigrade. Such a limiting chip case temperature is not unreasonable for commercial components; some of the commercial components analyzed in Reference 1 operated with case temperatures as high as 85 degrees centigrade.

The temperature predictions for the "radiation only" situation was based, essentially, on the circuit board/heat sink arrangement shown in Figure 13. The predictions are hypothetical because it may be very difficult to make the design shown in Figure 13 a reality.

It is possible to estimate the maximum error in the predicted chip temperatures that would results if the discrepancy between measured and calculated PC104 power dissipation were ignored. As an example consider the following: the thermal math model for the "radiation only" situation was run with 19% more dissipation on the large hot chip (chip A) on the VGA board. 19% is the magnitude of the total board dissipation discrepancy or error (0.6 watts/3.2 watts). The result was a 9 degree increase in the chip's predicted temperature: from 67 degrees centigrade to 76 degrees centigrade. While a substantial increase, it is also probably too large since it assumes that the chips not represented by heater nodes (i.e. lower dissipators such as memory chips) dissipate zero power. If, instead, we increase the VGA chip A dissipation by only 10%, a more likely estimate of the error in that chip's calculated dissipation, then the prediction for that chip increases by only 4 degrees centigrade.

CONCLUSIONS & RECOMMENDATIONS

The analysis of the WinSystems PC104 COTS boards through testing and thermal math modeling has yielded measured versus predicted temperature correlations that are typically within 2 or 3 degrees centigrade. As a means of determining the thermal characteristics of COTS boards and their suitablity for space flight applications, the method herein described can be applied with a reasonably high expectation of success. Also, if the configuration shown in Figure 13 can be realized, the subject COTS boards should be able to operate in a vacuum.

Certain improvements to the method are, however, recommended for any future COTS board tests and analyses. While it appears that the error in the analyses of these boards was rather low, it cannot be assumed that other boards with other chip configurations will be as tolerant of the large variation of heat transfer coefficient that was seen in this analysis. Consequently, future tests set-ups should allow the top surface of the boards to be subjected either to slowly developing flow, or flow that is completely developed, such as would exist at the downstream end of a plate or downstream of the entrance region of a duct. Ideally, the board should be part of the duct or plate surface over which the air is flowing; this would reduce the chance of flow separation and preclude the need for a "streamliner". "Streamliners" can introduce error because they tend to make an airfoil out of the board, increasing the speed of the air near the board with respect to the free stream air. In this test, the effect was estimated to influence temperatures by, at most, only 1 to 1.5 degrees centigrade, therefore it was ignored. On the other hand if the "streamliner" were larger and if, in addition, it were used in a small duct, the effect would be more serious.

Instrumentation, like a hot wire anemometer, would aid in the assessment of flow irregularities by allowing measurement of air speed over or around smaller scale structures. Provided that board surface emittances can be measured *and that they are fairly constant over the surface of a board*, an IR camera should be used to monitor and record temperatures. Thermocouples require substantial amounts of work to install, and if

they are too thick, can introduce heat leaks (i.e. error) from the chips; on the other hand, thin thermocouples are susceptible to electromagnetic interference.

Over a range of air speeds, the temperature of the free stream air should be maintained as constant as possible. In this test that was not possible. The work input of the rather large fan motor was sufficient to substantially raise the temperature of the air at the higher air speeds. If the air temperature gets too high, there is the possiblity of chip failure due to overheating. Also, high air temperature means the effective introduction of another heat source, enabling heat to flow from the hot air to cooler areas of the board; potentially increasing the analytical error. In general, thermally isolating a board under test from any other heat sources, including other boards (which may need to operate simultaneously with the board under test), is desirable.

While very good results were obtained in this effort by modeling with SINDA85, a computational fluid dynamics (CFD) program geared to circuit board thermal analyses would provide more accuracy in situations where board or other flow influencing geometry is complex. Such CFD packages use graphics interfaces to facilitate modeling, and some have the ability to import existing CAD geometries, a capability which would further reduce the modeling effort. Furthermore, if COTS boards analysis became especially frequent (about one every several months), the economics of purchasing a CFD package should be favorable.

REFERENCES

1. Thermal Accommodation of Commercial, Off-the Shelf (COTS) Boards in the Central Unit Electronics (CUE) Box of the Spartan 251 Spacecraft, SAI-RPT-292 Rev -; F. Giacobbe, 30 August 1999

2. COTS Boards Insertion Methodology and Plan, J. Plante, C. Eveland, N. Helmhold, M. Gates, B. Settles, G. Martins, August 1998

FIGURES

FIGURE 1 - SET-UP FOR PC104 CONNECTION HEAT TRANSFER TEST

(DUCT TAPE ENCLOSING TWO LOWER BOARDS NOT SHOWN, SEE FIG 2)

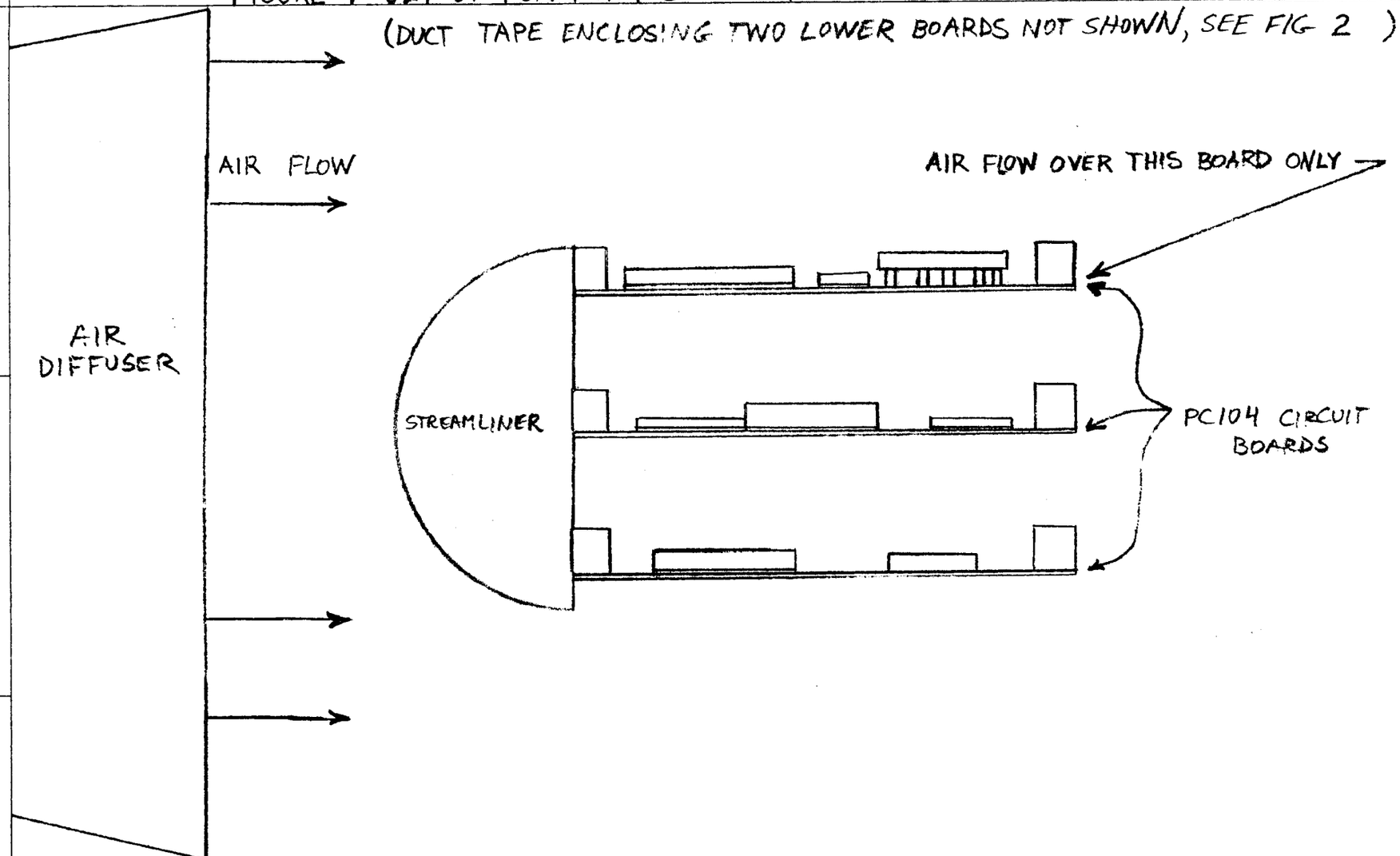


FIGURE 2-- PC104 CONVECTION HEAT TRANSFER TEST

FIGURE 3- IR IMAGE OF VERTICALLY MOUNTED PROCESSOR BOARD

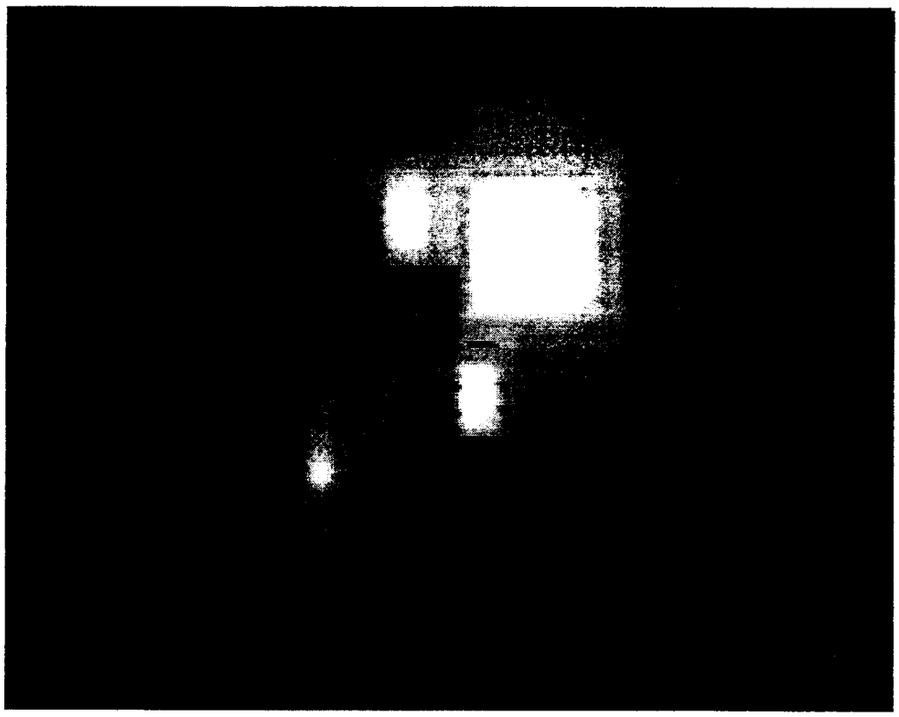


FIGURE 4- IR IMAGE OF VERTICALLY MOUNTED I/O BOARD

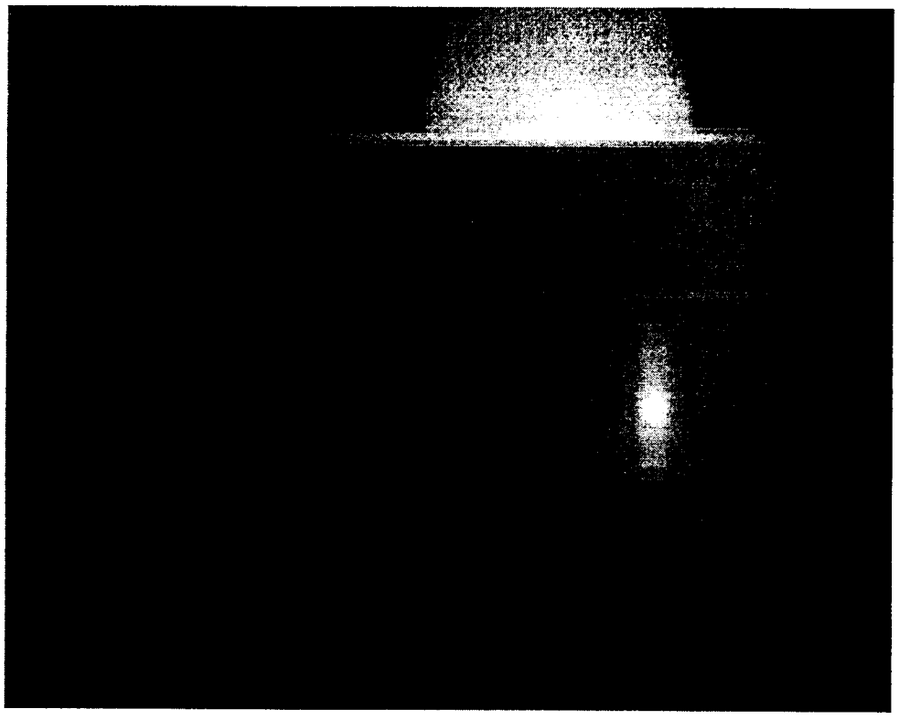
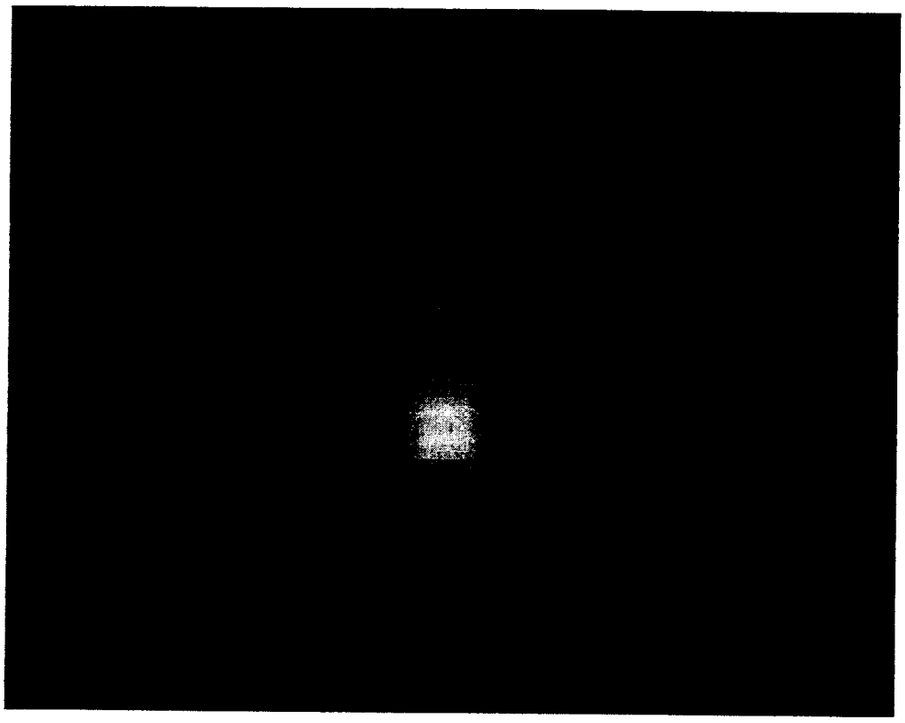
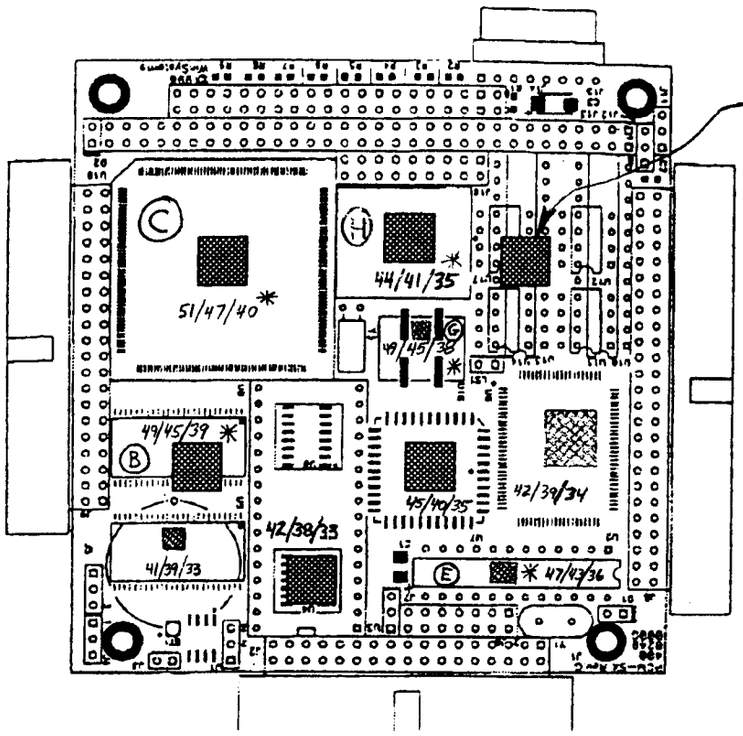


FIGURE 5- IR IMAGE OF VERTICALLY MOUNTED VGA BOARD



FURE 6A - MEASURED PROCESSOR BOARD TEMPERATURES IN FORCED CONVECTION (DEG C)



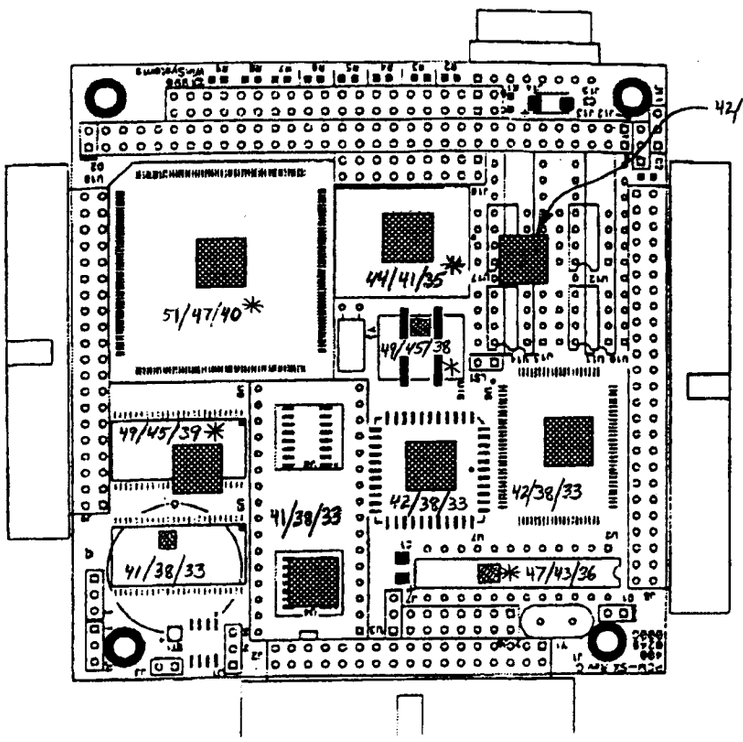
LEGEND (FOR BOTH FIGURES)

▨ = LOCATION OF TEMP. MEASUREMENT

T1/T2/T3 = TEMP @ 4 m.per.sec / TEMP @ 7 m.per.sec / TEMP @ 15 m.per.sec.

✳ = HEATER NODE (IN TMM)

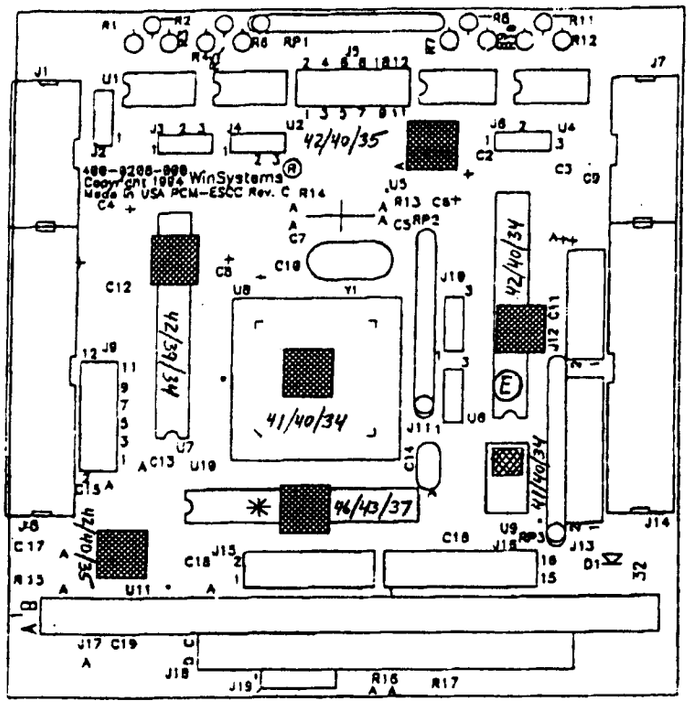
GURE 6B - CALCULATED PROCESSOR BOARD TEMPERATURES IN FORCED CONVECTION (DEG C)



NOTES (FOR BOTH FIGURES)

- T_{air} = 43/38/33 °C
- T_{room} = 22/23/24 °C
- IN TMM, HEATER NODES MAINTAINED @ MEASURED TEMP. TO DETERMINE THEIR POWER DISSIPATION.

FIGURE 7A - MEASURED I/O BOARD TEMPERATURES IN FORCED CONVECTION (DEG C)



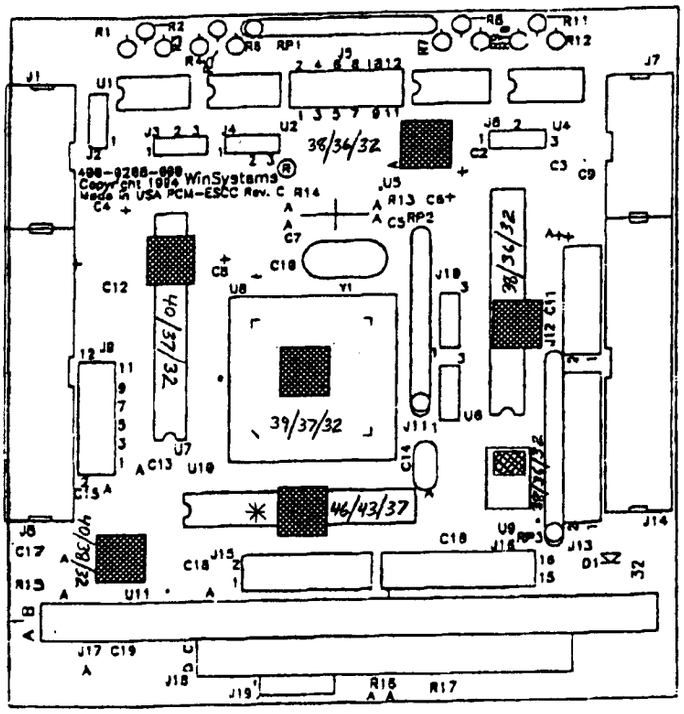
LEGEND (FOR BOTH FIGURES)

▩ = LOCATION OF TEMP. MEASUREMENT

T1/T2/T3 = TEMP @ 4 m. per. sec / TEMP @ 7 m. per sec / TEMP @ 15 m. per sec.

✳ = HEATER NODE (IN TMM)

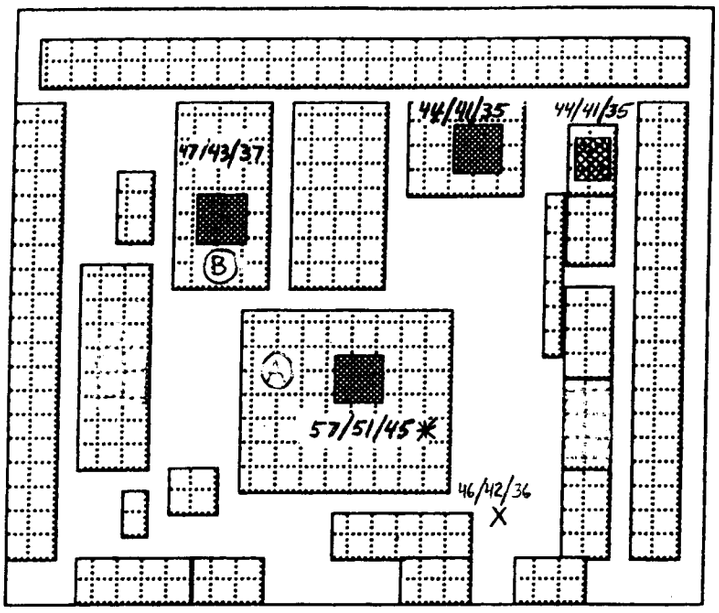
FIGURE 7B - CALCULATED I/O BOARD TEMPERATURES IN FORCED CONVECTION (DEG C)



NOTES (TYP BOTH FIGURES)

- T_{air} = 42/39/33 °C
- T_{room} = 22/23/24 °C
- IN TMM, HEATER NODES MAINTAINED @ MEASURED TEMP. TO DETERMINE THEIR POWER DISSIPATION.

FIGURE 8A - MEASURED VGA BOARD TEMPERATURES IN FORCED CONVECTION (DEG C)



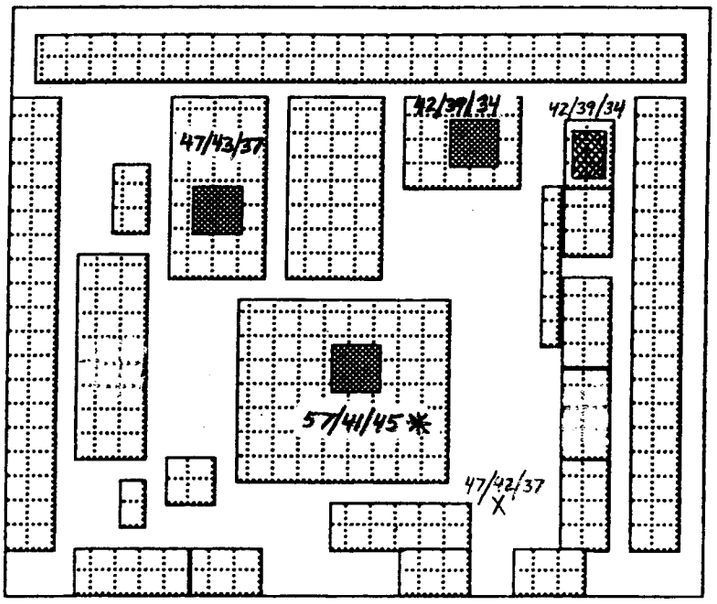
LEGEND (FOR BOTH FIGURES)

▩ = LOCATION OF TEMP. MEASUREMENT

T1/T2/T3 = TEMP @ 4 m. per sec / TEMP @ 7 m. per sec / TEMP @ 15 m. per sec.

✳ = HEATER NODE (IN THM)

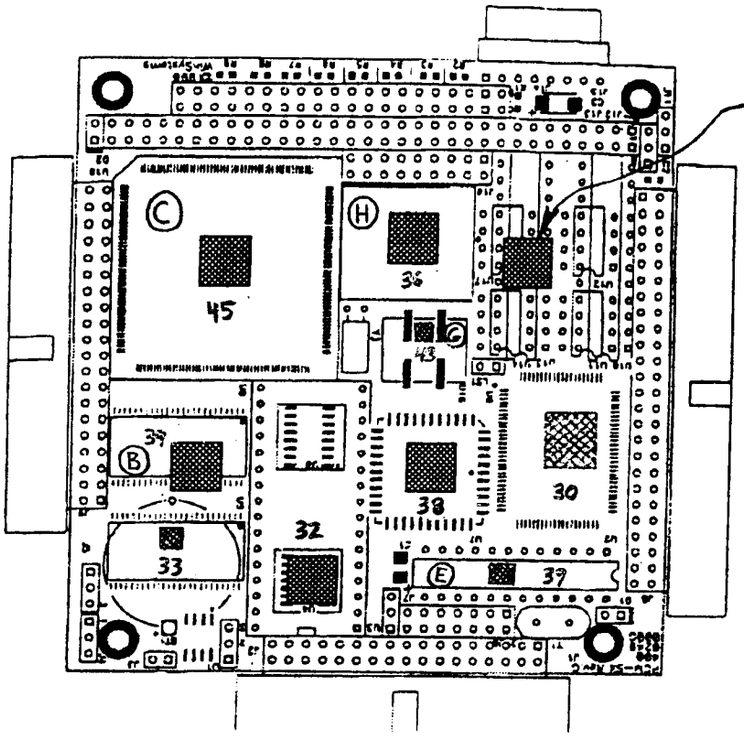
FIGURE 8B - CALCULATED VGA BOARD TEMPERATURES IN FORCED CONVECTION (DEG C)



NOTES (TYP BOTH FIGURES)

- T_{air} = 44/40/34 °C
- T_{room} = 22/23/24 °C
- IN THM, HEATER NODES MAINTAINED @ MEASURED TEMP. TO DETERMINE THEIR POWER DISSIPATION.

FIGURE 9A - MEASURED PROCESSOR BOARD TEMPERATURES IN NATURAL CONVECTION (DEG C)

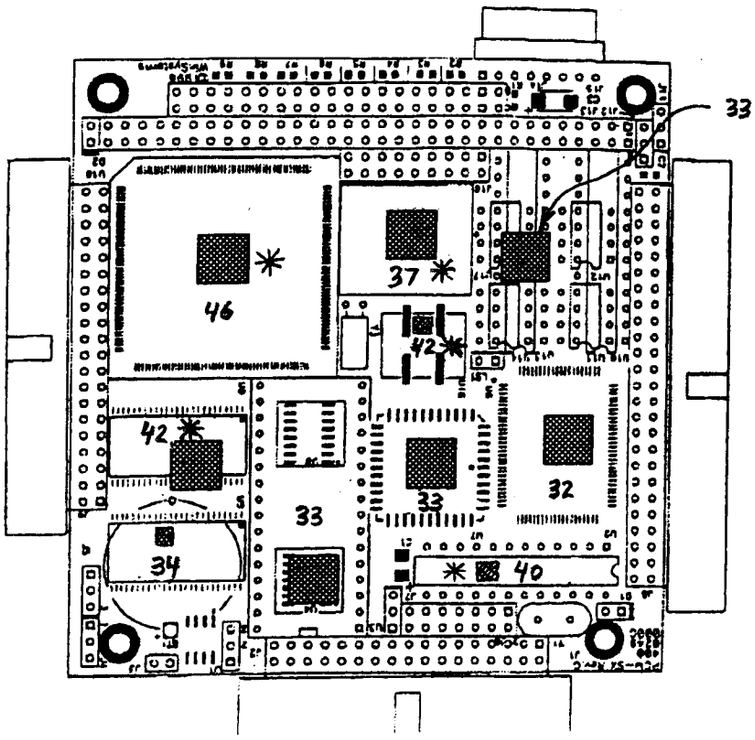


LEGEND (FOR BOTH FIGURES)

▩ = LOCATION OF TEMP. MEASUREMENT

✳ = POWER DISSIPATING NODE

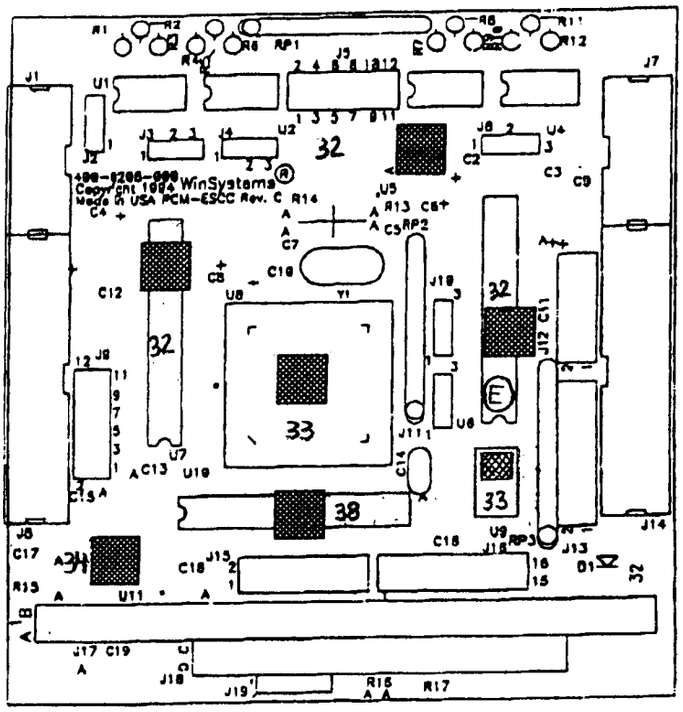
FIGURE 9B - CALCULATED PROCESSOR BOARD TEMPERATURES IN NATURAL CONVECTION (DEG C)



NOTES (FOR BOTH FIGURES)

- T_{room} = 22/23/24 °C
- HEAT LOAD DETERMINED IN FORCED CONVECTION CORRELLATION IMPOSED ON POWER DISSIPATING NODES.

FIGURE 10A - MEASURED I/O PROCESSOR BOARD TEMPERATURES IN NATURAL CONVECTION (DEG C)

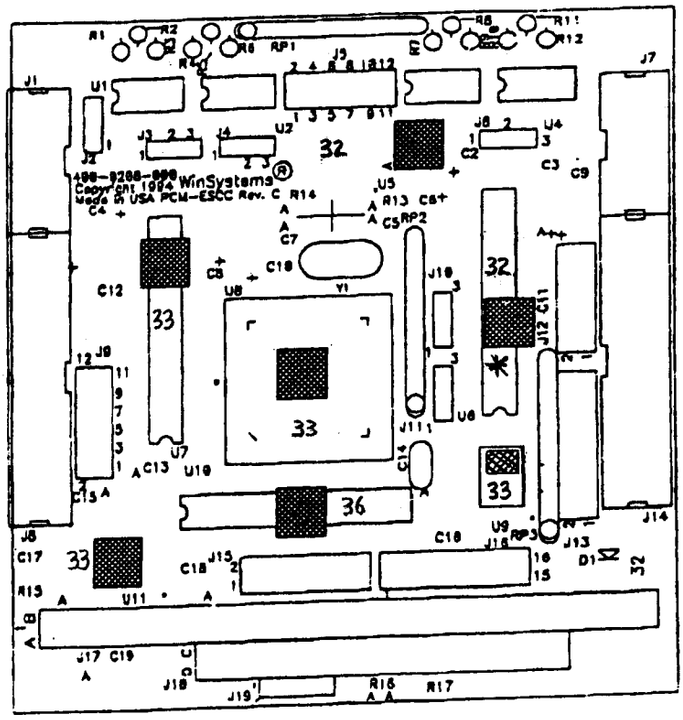


LEGEND (FOR BOTH FIGURES)

▩ = LOCATION OF TEMP. MEASUREMENT

✳ = POWER DISSIPATING NODE

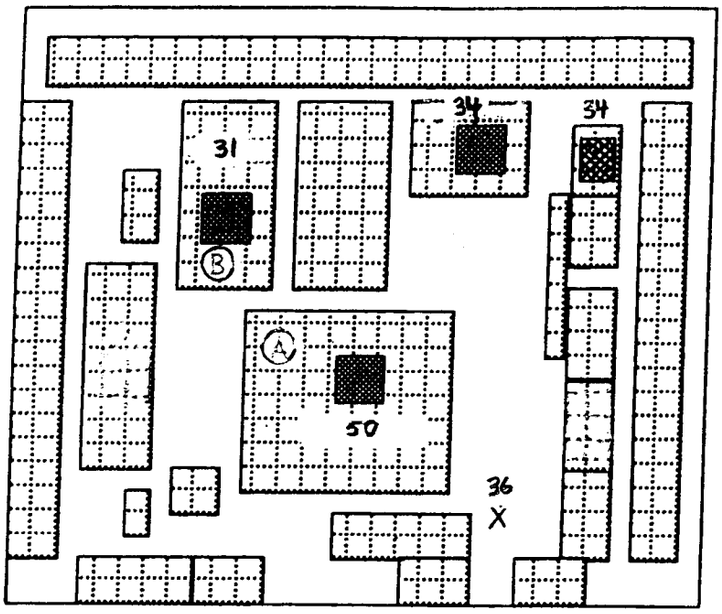
FIGURE 10B - CALCULATED I/O BOARD TEMPERATURES IN NATURAL CONVECTION (DEG C)



NOTES (FOR BOTH FIGURES)

- T_{room} = 22/23/24 °C
- HEAT LOAD DETERMINED IN FORCED CONVECTION CORRELLATION IMPOSED ON POWER DISSIPATING NODES

FIGURE IIA - MEASURED VGA BOARD TEMPERATURES IN NATURAL CONVECTION (DEG C)

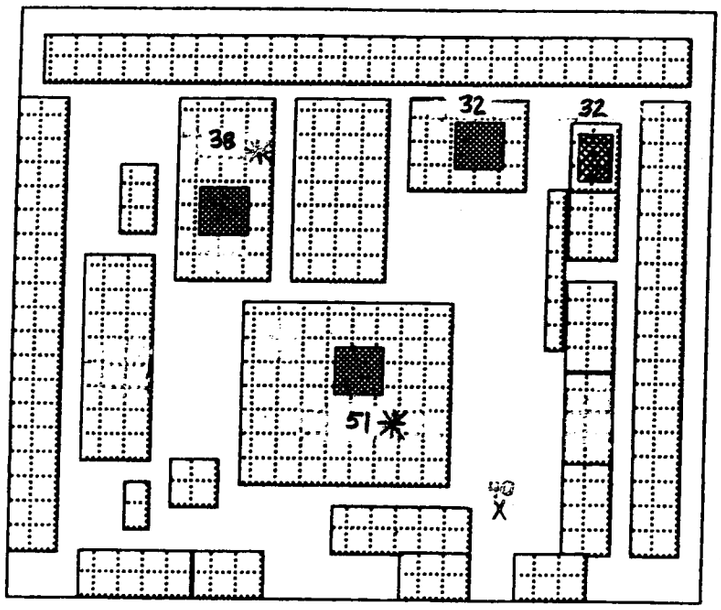


LEGEND (FOR BOTH FIGURES)

▩ = LOCATION OF TEMP. MEASUREMENT

✳ = POWER DISSIPATING NODE

FIGURE IIB - CALCULATED VGA BOARD TEMPERATURES IN NATURAL CONVECTION (DEG C)



NOTES (FOR BOTH FIGURES)

- T_{room} = 22/23/24 °C
- HEAT LOAD DETERMINED IN FORCED CONVECTION CORRELLATION IMPOSED ON POWER DISSIPATING NODES

FIGURE 12A-TEMPERATURE PREDICTIONS FOR PROCESSOR BOARD WITH RADIATIVE HEAT REJECTION ONLY

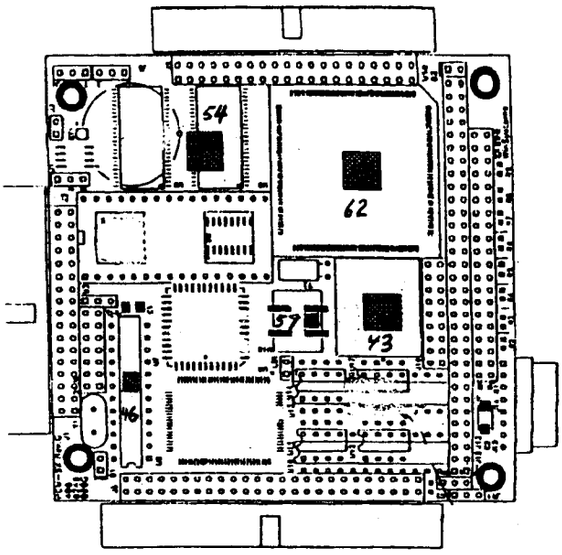
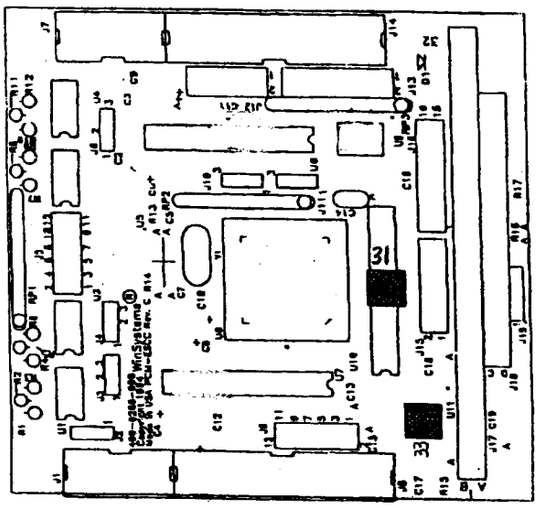
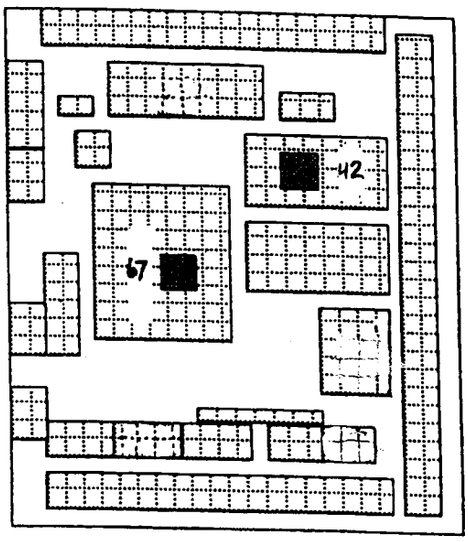


FIGURE 12B-TEMPERATURE PREDICTIONS FOR I/O BOARD WITH RADIATIVE HEAT REJECTION ONLY



IGURE 12C-TEMPERATURE PREDICTIONS FOR VGA BOARD WITH
ADIATIVE HEAT REJECTION ONLY



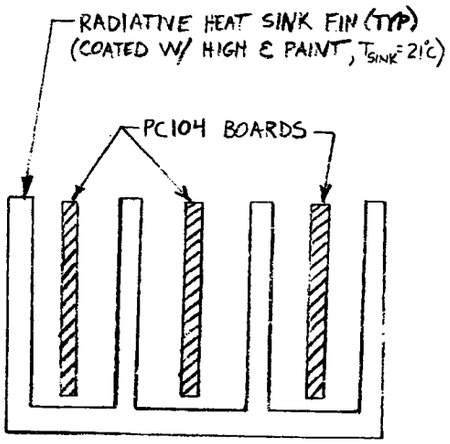


FIGURE 13-RADIATIVE HEAT SINK CONCEPT FOR PC104 BOARDS

TABLES

TABLE 1 - CALCULATED POWER DISSIPATION OF PC104 BOARD COMPONENTS (WATTS)

	COMPONENT DESIGNATION	POWER DISSIPATION (W) Vair = 4m/s	Vair = 7m/s	Vair = 15 m/s
PROCESSOR BOARD				
	C	0.82	0.91	0.91
	B	0.24	0.25	0.23
	E	0.2	0.23	0.16
	G	0.19	0.21	0.17
	H	0.03	0.05	0.04
I/O BOARD				
	E	0.07	0.12	0.08
VGA BOARD				
	A	1.37	1.24	1.39
	B	0.16	0.15	0.15
TOTAL		3.09	3.17	3.13

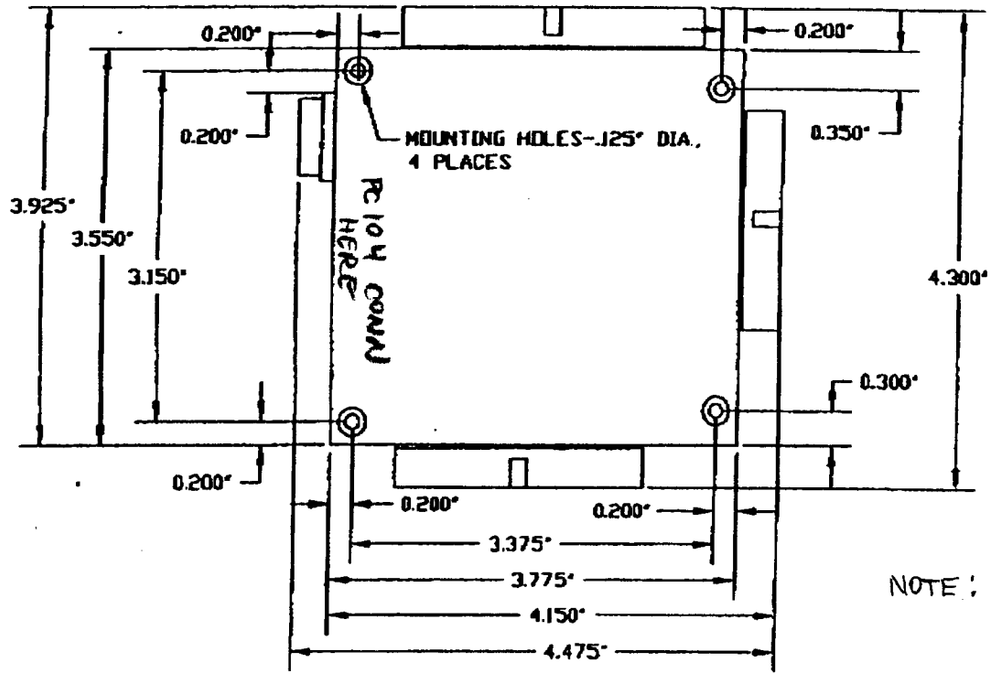
* See Figures 6a, 7a, & 8a for loaction of components.

MEASURED TOTAL = 3.76

Appendix A

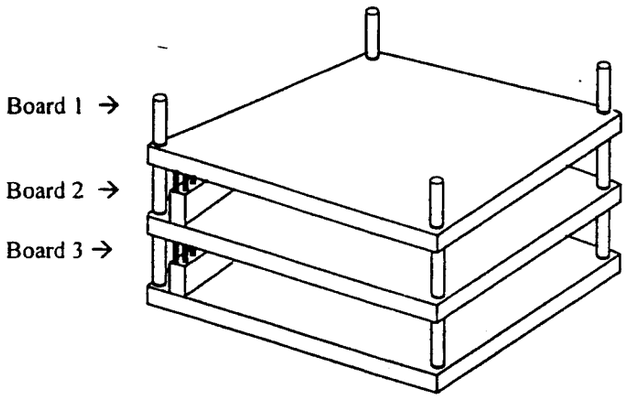
COTS Board & PC104 Computer Dimensions

REVISIONS			
REV.	DESCRIPTION	DATE	CHANGED BY



NOTE: DIMENSIONS SAME FOR PROCESSOR, I/O, VGA BOARDS.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE FRACTIONS ANGLES +/- 1/2° DECIMALS .XX ± .03 .XXX ± .010	DRAFT/DESIGN M.BROWNING	DATE 10-10-96	*WinSystems, Inc.* "THE STD BUS AUTHORITY"
	CHECKER	DATE	
MACHINE FINISH ✓	APPROVAL	DATE	PCM-SX, CPU PHYSICAL, MOUNTING DETAILS
	CUSTOMER APPROVAL	DATE	SIZE B · CAGE CODE 14687 · DWG NO. PCMSXMEC.DWG · REV A · CAD ID: [illegible] · SHEET 1 OF 1



Boards, standoffs and inter-board connectors shown. Components not shown. Dimensions are 3.6 x 3.8 x 2.5 inches

PC104 COMPUTER DIMENSIONS

Appendix B

Corrected IR tempeartures, Measured IR Temperatures, & Chip Letter Designations

IR CAMERA TEMPERATURES (C)				
	COMP. NAME	MEASURED	CORRECTED MEAS.	PREDICTION
PROCESSOR BOARD				
	A	28	22	33
	B	51	41	41
	C	56	46	45
	D	36	26	31
	E	46	36	38
	F	40	30	32
	G	48	38	40
	H	38	28	36
	I	32	23	31
	J	36	26	32
	K	34	25	30
I/O BOARD	A	32	22	24
	B	34	24	24
	C	31	22	24
	D	33	23	25
	E	43	33	29
	F	31	22	24
	G	34	24	25
VGA BOARD	A	64	54	56
	B	41	31	36
	C	33	24	29
	D	33	23	28

BLDG 5 RM C232 PALAYA;
PICK UP SIGNED LIST DATA FORM.
TAKE LIST TO SECURITY IN GATEHOUSE
OF BLDG 9.

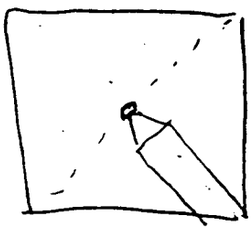
WANDA PETERS X 5147
BLDG 7, RM 12 (DOWNSTAIRS)

CHARGE NO 2103-T94

SILICONE EMISSIVITY ≈ .7
PLASTIC EMISSIVITY ≈ .8

GALILEO

1) LOCATE TC AT CENTER PT OF CHIP



2)

16 NOV 99
18 AUG 99

VGA BOARD

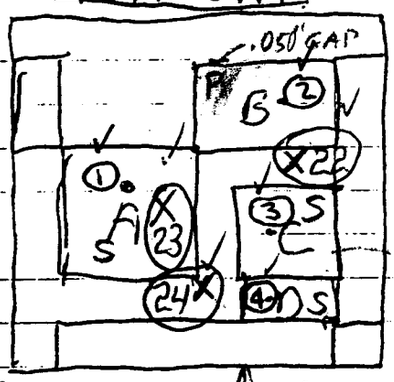
VGA BOARD

		FILE#
A:	~~68.1~~ C	1/2
B.	40.7 C	3/4
C.	33.3 C	5/6
~~D. 32.7 C~~		7/8

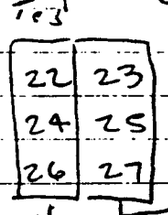
~~,23~~ 24 Board (where you can)

~~NOTE:~~

1. A HEATS BOARD UP
2. WITHOUT A, BOARD IS ISOTHERMAL/I.E. UNIFORM TEMPERATURE SURFACE - BOARD IN POWER CONV MODE.



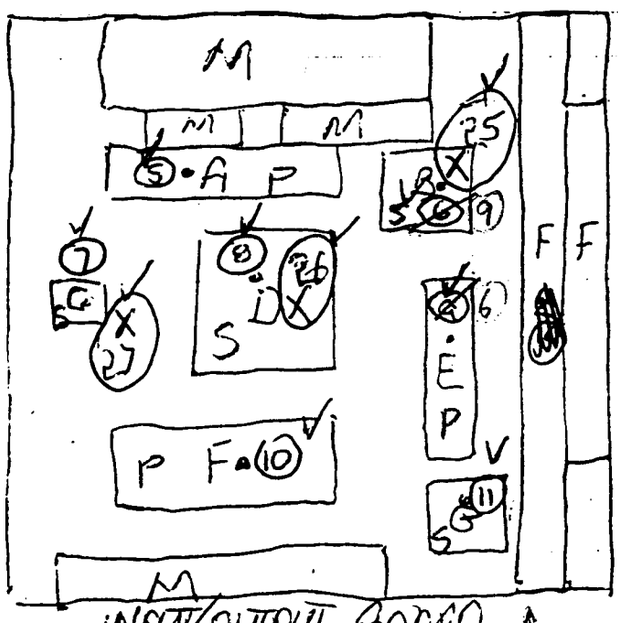
NOTE: EVEN # B/I
ODD # COLD



I/O BOARD

		FILE#
A =	31.7 C	1/2
B =	33.5 C	3/4
C =	31.1 C	5/6
D =	32.5 C	7/8
E =	42.5 C	9/10
F =	31.4 C	11/12
G =	33.8 C	13/14

~~25~~ 26, 27 Board (where you can)



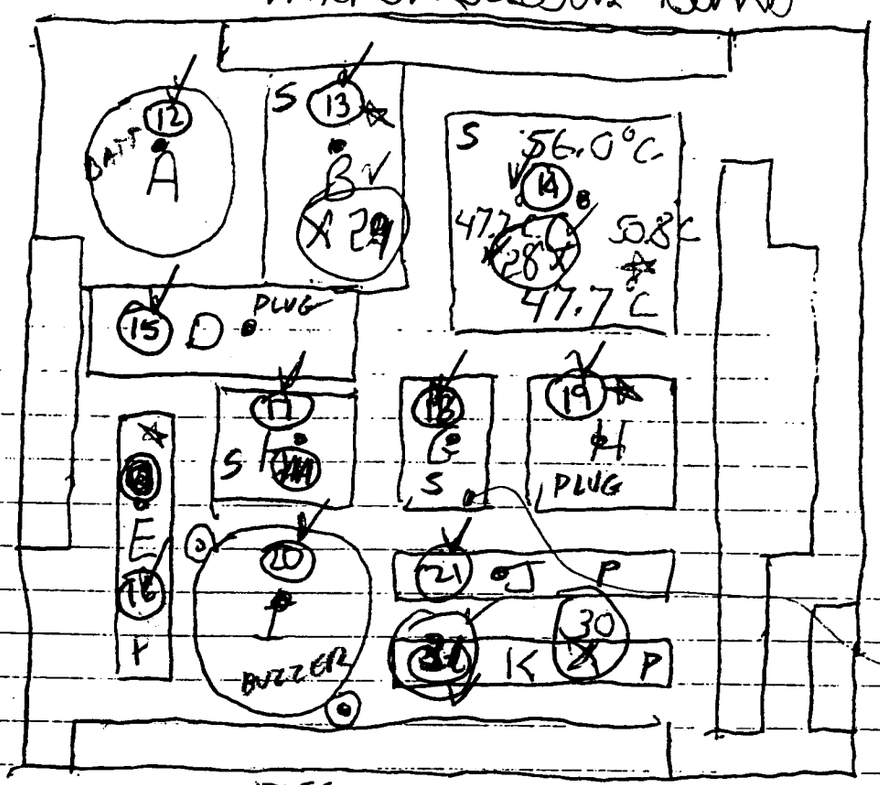
KAPTON TAPE THICKNESS = .002" / LAYER
2 LAYERS TOTAL

34

10 AUG 90

3. ~~UP BOARD~~:

MICROPROCESSOR BOARD



		WIRES
12	A: 27.8 °C	1/2
13	B: 51.1 °C	3/4
14	C: 56.3 °C	5/6
15	D: 35.6 °C	7/8
16	E: 45.7 °C	9/10
17	F: 39.5 °C	11/12
18	G: 48.1 °C	13/14
19	H: 38.0 °C	15/16
20	I: 32.4 °C	17/18
21	J: 36.0 °C	19/20
~~31~~	K: 34.1 °C	21/22

AIR

28
29
30

~~26, 27~~ Board
28, 29, 30

Appendix C

Temperatures Recorded During Convective Tests at the Glenn L. Martin Facility

(Nov. 1999)

CHIP NODE #

TC #

STEADY STATE TEMPERATURES (°C)

BOARD ASSEMT		m/s AIR SPEED	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
																								VGA BOARD			I/O BOARD				PROC BOARD			HR TEMP
PROC	1158	0	40	38	34	33	36	41	35	36	35	36	35	33	39	45	32	38	38	42	36	20	34	35	40	34	35	35	34	39	37	34	33	22
I/O	1335	7.07	57	45	42	42	43	49	43	44	43	43	44	41	49	61	42	47	45	49	44	42	42	43	47	43	43	44	42	46	46	44	43	43
VGA	1015	7.07	42	42	39	38	40	45	39	40	40	40	41	39	45	47	38	42	40	45	41	39	40	40	42	40	40	40	39	43	41	41	40	38
	1151	15	46	37	33	33	34	40	34	35	34	34	35	33	39	40	33	36	35	38	35	34	35	35	37	35	34	34	34	36	36	35	34	33
I/O	1145	0	54	41	37	36	32	38	32	33	33	32	34	35	41	47	39	41	40	46	38	40	35	40	45	39	33	34	33	39	38	36	34	23
VGA	1262	4.47	59	47	45	45	42	46	42	42	41	42	42	42	49	53	44	48	48	52	44	46	43	45	50	46	42	42	41	45	43	42	43	42
PROC	1039	7.07	55	44	42	42	40	43	40	40	40	39	40	39	43	46	40	45	42	48	42	42	40	43	46	43	40	40	39	41	41	41	40	39
	1100	7.07 7.07	51	42	40	40	40	42	41	40	39	39	39	40	45	47	40	42	40	44	40	39	38	40	42	39	39	39	39	41	39	39	39	39
	1137	15	49	36	35	36	34	37	35	34	34	34	35	34	40	42	33	38	36	40	36	35	35	36	39	36	34	34	34	36	35	35	34	33
VGA	1157	0	50	31	34	34	33	39	31	33	33	32	32	37	45	48	39	43	42	48	39	39	36	37	42	36	33	36	38	41	40	37	37	24
PROC	1350	4.47	57	47	44	44	43	49	42	43	43	43	44	46	53	57	47	52	51	57	49	47	47	46	50	46	43	43	42	50	49	48	47	44
I/O	1126	7.07	51	43	41	41	40	46	40	41	41	40	41	41	48	53	43	48	47	53	46	44	44	42	45	42	40	40	39	46	44	44	43	40
	1155	7.07 7.07	51	42	40	40	41	43	40	40	40	40	40	41	47	49	40	44	42	45	42	40	40	40	43	40	39	40	39	43	42	41	40	40
	1538	15	45	37	35	35	35	39	35	35	36	35	35	35	42	45	36	40	39	45	38	37	37	36	38	36	35	35	35	38	38	38	37	34

Appendix D

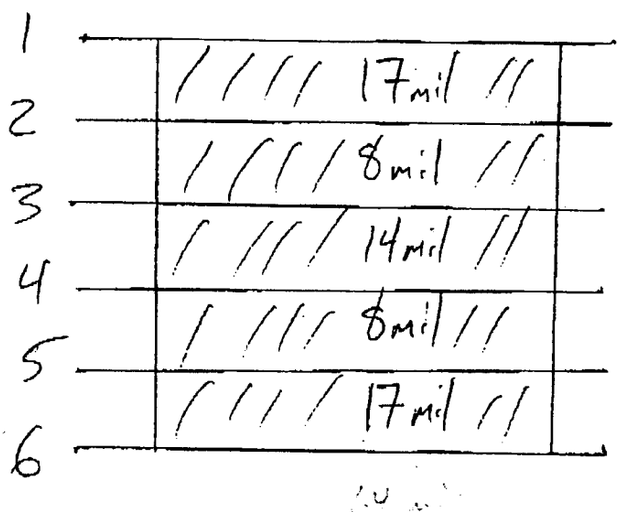
Thickness of Copper Strata in PC104 Boards

Project file name: c:\000\cam\~win0234d\cam350-win0234d.pcb
Date: Mon Nov 8 10:59:55 1999

Layer Name	Copper On Layer Sq In	Copper In Holes Sq In	Total Copper
1:1top	2.9725	2.0866	5.0590
2:2sig	1.9419	0.0000	1.9419
3:3gnd	2.2474	0.0000	2.2474
4:4pwr	2.3272	0.0000	2.3272
5:5sig	1.3091	0.0000	1.3091
6:6bot	1.8031	2.0866	3.8897
~~12:drill.ext~~	~~0.0000~~	~~0.0000~~	~~0.0000~~
Totals:	12.6012	4.1731	16.7743

Copper in holes is 1 mil Thick

0234 rev. D



1.7 mils Cu $\times \frac{2.97}{(3.55)(3.775)} = 0.222$ in.
1.4 mils Cu $\times \frac{1.94}{(3.55)(3.775)} = 0.203$
1.4 mils Cu $\times \frac{2.25}{(3.55)(3.775)} = 0.235$
1.4 mils Cu $\times \frac{2.33}{(3.55)(3.775)} = 0.243$
1.4 mils Cu $\times \frac{1.31}{(3.55)(3.775)} = 0.177$
1.7 mils Cu $\times \frac{1.80}{(3.55)(3.775)} = 0.248$

TTL. EFF. THK = 1.268 in.

$G_{G10} = \frac{(0.3)(.236)^2(.0254)^3}{.064/2} = 0.0132$ W/°C ≈ 13.5X LARGER THAN FORCED CONVECTION

= dielectric $G_{\text{COPPER}} = \frac{382(.236)(.00127)(.0254)}{.236} = 0.0123 \frac{W}{°C}$

VGA card.

$G_{G\text{-}10} = \frac{(0.3)(.236)(.064)(.0254)}{0.236}$

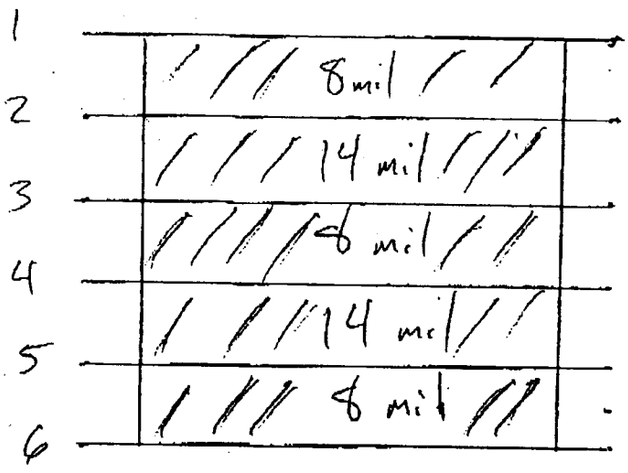
= .000488 (NEGLIGIBLE)

Project file name: c:\000\cam\win0249j\cam350-win0249j.pcb
Date: Mon Nov 8 09:59:14 1999

0249 Rev J

Layer Name	Copper On Layer Sq In	Copper In Holes Sq In	Total Copper
1:1top	3.2091	2.3251	5.5342
2:2pwr	3.5995	0.0000	3.5995
3:3sig	3.1169	0.0000	3.1169
4:4sig	3.1227	0.0000	3.1227
5:5gnd	3.4943	0.0000	3.4943
6:6bot	3.1983	2.3251	5.5233
Totals:	19.7409	4.6502	24.3910

Copper in holes is 1 mil Thick



EFFECTIVE THICKNESS

1.7 mils Cu $\times \frac{3.21}{(3.55)(3.775)}$ = 0.407 mils

1.4 mils Cu $\times \frac{3.60}{(3.55)(3.775)}$ = 0.376

1.4 Mils Cu $\times \frac{3.12}{(3.55)(3.775)}$ = 0.233

1.4 Mils Cu $\times \frac{3.12}{(3.55)(3.775)}$ = 0.233

1.4 Mils Cu $\times \frac{3.49}{(3.55)(3.775)}$ = 0.367

1.7 Mils Cu $\times \frac{3.30}{(3.55)(3.775)}$ = 0.446

TOTAL EFF THK = 2.02 mils

= dielectric $\frac{(382)(.236)(.0002)/.0254}{1.236}$

= 0.019 W/°C

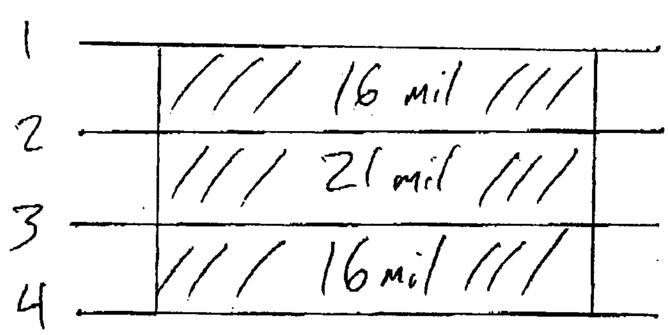
µProcessor card

Project file name: c:\000\cam\~win0208c\cam350-win0208c.pcb
Date: Mon Nov 8 10:40:37 1999

Layer Name	Copper On Layer Sq In	Copper In Holes Sq In	Total Copper
1:1top	1.8636	1.8945	3.7582
L2:2gnd	2.0339	0.0000	2.0339
L3:3pwr	2.0864	0.0000	2.0864
L4:4bot	1.3585	1.8945	3.2530
~~E10:drill.txt~~	~~0.0000~~	~~0.0000~~	~~0.0000~~
Totals:	7.3425	3.7891	11.1316

~~0208~~ rev. C
0208

Copper in holes is 1 mil Thick



EFF. THK.

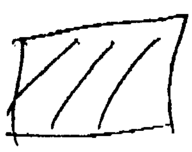
2.4 mils Cu × $\frac{1.86}{(3.55)(3.775)}$ = 0.333 m

1.4 mils Cu × $\frac{2.03}{(3.55)(3.775)}$ = 0.212

1.4 mils Cu × $\frac{2.09}{(3.55)(3.775)}$ = 0.218

2.4 mils Cu × $\frac{1.36}{(3.55)(3.775)}$ = 0.244

TTL. EFF THK. 1.007 mils

 = dielectric

$G_{\text{MAX THRU COPPER}} = \frac{(382)(.236)(.00101)(.0244)}{.236}$

= 0.0098 W/°C

I/O board

Appendix E

SINDA85 Nodal Diagrams & Model

CPU PCB

ASSY

JF-2P

J6

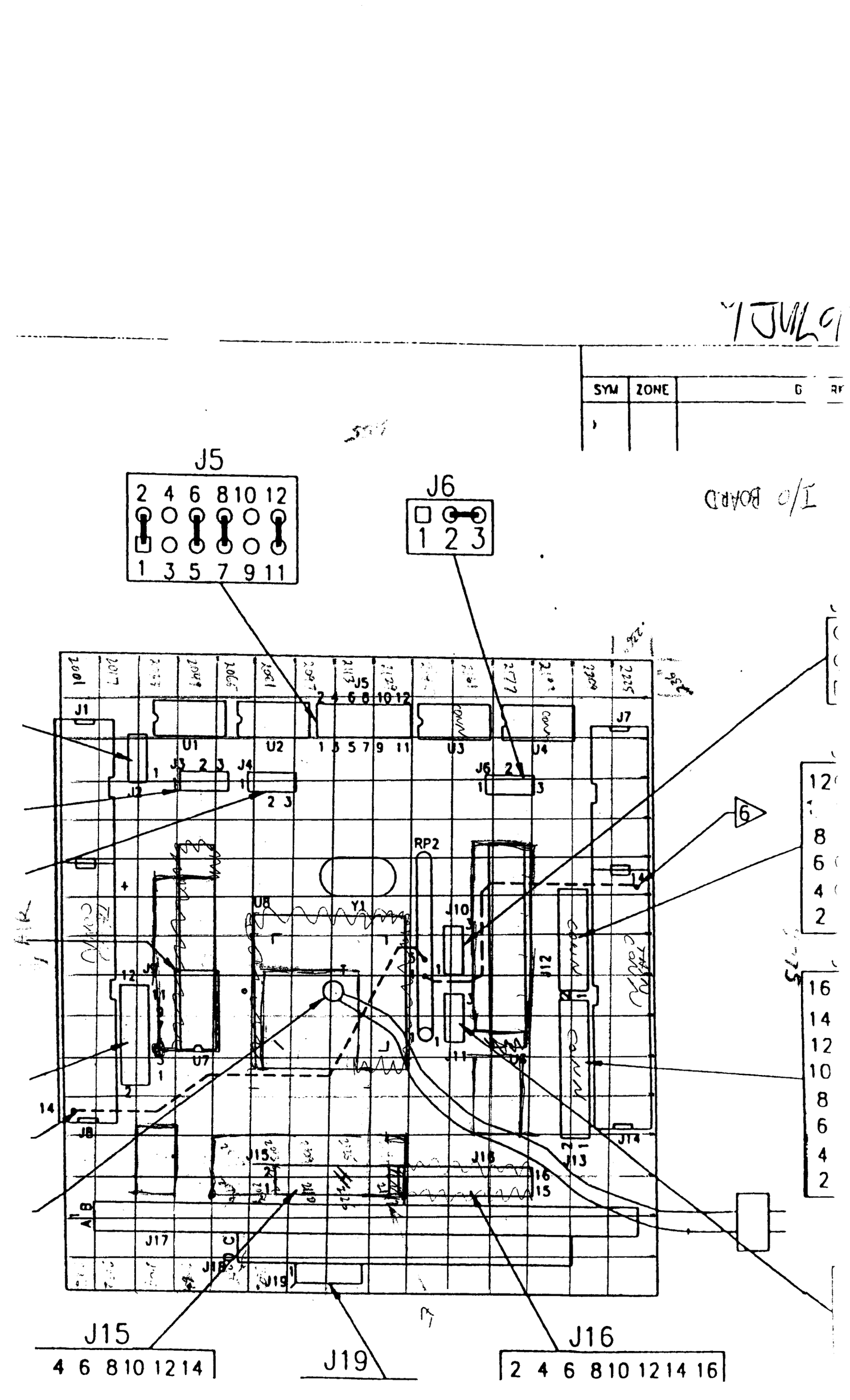
J12

J11

J10

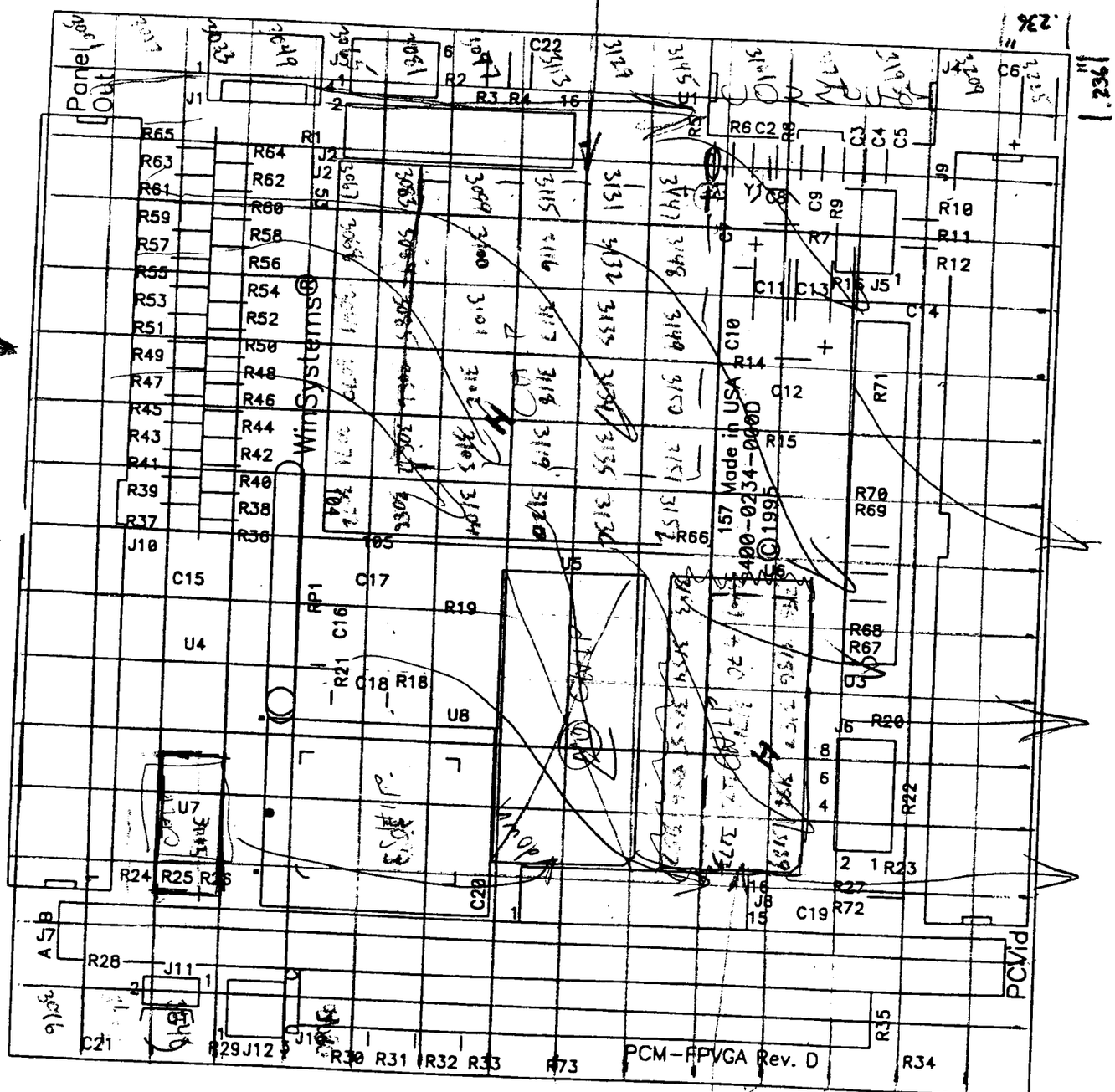
5

6


J5
2 4 6 8 10 12
1 3 5 7 9 11
J6
1 2 3
U1
U2
U3
U4
U7
U8
RP2
Y1
J1
J2
J3
J4
J7
J8
J10
J11
J12
J13
J14
J15
J16
J17
J18
J19
J15
4 6 8 10 12 14
J19
J16
2 4 6 8 10 12 14 16

3 APPENDIX A

PCM-FPVGA Parts Placement Guide



CONV3.INP

```
ADER OPTIONS DATA
TLE   CORRELATION MODEL FOR U OF MD PC104 COTS BOARD LAMINAR FLOW COOLING TEST
      MODEL = COTS
       OUTPUT = CONV417.OUT
      OUTPUT = TEST.OUT

ADER CONTROL DATA, GLOBAL
      UID = SI
      ABSZRO = -273.15
      SIGMA = 5.67E-08
      NLOOPS = 20000
      ARLXCA = 0.0001
      EBALSA = 0.0001

ADER USER DATA, GLOBAL

    DEFINE CONVECTION CONTANTS

       THE VALUE OF A CONVECTION COEFFICIENT VARIES ONLY IN THE DOWNSTREAM DIRECTION.

       PC BOARD, TOP
       H1001=1.,H1002=1.,H1003=1.,H1004=1.,H1005=1.,H1006=1.,H1007=1.
       H1008=1.,H1009=1.,H1010=1.,H1011=1.,H1012=1.,H1013=1.,H1014=1.,H1015=1.
       H1016=1.


       VAIR = 4.17
       ANODE = 0.236*0.236*0.0254*0.0254

       QTOT = 0., QCPROC =0., QBPROC =0., QEPROC=0., QGPROC=0., QHPROC=0.
       QEIO=0.,   QAVGA=0.,   QBVGA=0.

EADER NODE DATA, PCB


NCLUDE NDAT417.DAT
INCLUDE NDAT707.DAT
INCLUDE NDAT150.DAT


EADER CONDUCTOR DATA, PCB

********************** CPU **********************
   PCB
      BOARD X-DIRECTION

      GEN   1, 15, 1, 1001, 1, 1002, 1, 0.019
      GEN  16, 15, 1, 1017, 1, 1018, 1, 0.019
      GEN  31, 15, 1, 1033, 1, 1034, 1, 0.019
      GEN  46, 15, 1, 1049, 1, 1050, 1, 0.019
      GEN  61, 15, 1, 1065, 1, 1066, 1, 0.019
      GEN  76, 15, 1, 1081, 1, 1082, 1, 0.019
      GEN  91, 15, 1, 1097, 1, 1098, 1, 0.019
      GEN 106, 15, 1, 1113, 1, 1114, 1, 0.019
      GEN 121, 15, 1, 1129, 1, 1130, 1, 0.019
      GEN 136, 15, 1, 1145, 1, 1146, 1, 0.019
      GEN 151, 15, 1, 1161, 1, 1162, 1, 0.019
      GEN 166, 15, 1, 1177, 1, 1178, 1, 0.019
      GEN 181, 15, 1, 1193, 1, 1194, 1, 0.019
```

```
      GEN 196, 15, 1, 1209, 1, 1210, 1, 0.019
      GEN 211, 15, 1, 1225, 1, 1226, 1, 0.019

      BOARD Y-DIRECTION

      GEN  301, 14, 1, 1001, 1, 1017, 1, 0.019
      GEN  315, 14, 1, 1017, 1, 1033, 1, 0.019
      GEN  329, 14, 1, 1033, 1, 1049, 1, 0.019
      GEN  343, 14, 1, 1049, 1, 1065, 1, 0.019
      GEN  357, 14, 1, 1065, 1, 1081, 1, 0.019
      GEN  371, 14, 1, 1081, 1, 1097, 1, 0.019
      GEN  385, 14, 1, 1097, 1, 1113, 1, 0.019
      GEN  399, 14, 1, 1113, 1, 1129, 1, 0.019
      GEN  413, 14, 1, 1129, 1, 1145, 1, 0.019
      GEN  427, 14, 1, 1145, 1, 1161, 1, 0.019
      GEN  441, 14, 1, 1161, 1, 1177, 1, 0.019
      GEN  455, 14, 1, 1177, 1, 1193, 1, 0.019
      GEN  469, 14, 1, 1193, 1, 1209, 1, 0.019
      GEN  483, 14, 1, 1209, 1, 1225, 1, 0.019

   CHIP X -DIRECTION

      GEN 500, 2, 1, 91089, 16, 91090, 16, 10.

      GEN 502, 2, 1, 91108, 16, 91109, 16, 10.

      GEN 504, 3, 1, 91182, 16, 91183, 16, 10.

      GEN 507, 4, 1, 91154, 1, 91155, 1, 10.
      GEN 511, 4, 1, 91170, 1, 91171, 1, 10.
      GEN 515, 4, 1, 91186, 1, 91187, 1, 10.
      GEN 519, 4, 1, 91202, 1, 91203, 1, 10.
      GEN 523, 4, 1, 91218, 1, 91219, 1, 10.

    CHIP Y-DIRECTION

      GEN 527, 4, 1, 91019, 16, 91035, 16, 10.

      GEN 531, 2, 1, 91089,  1, 91105,  1, 10.

      GEN 533, 2, 1, 91108,  1, 91124,  1, 10.

      GEN 535, 2, 1, 91182, 16, 91198, 16, 10.
      GEN 537, 2, 1, 91183, 16, 91199, 16, 10.

      GEN 5390, 4, 1, 91154, 16, 91170, 16, 10.
      GEN 5394, 4, 1, 91155, 16, 91171, 16, 10.
      GEN 5398, 4, 1, 91156, 16, 91172, 16, 10.
      GEN 5402, 4, 1, 91157, 16, 91173, 16, 10.
      GEN 5406, 4, 1, 91158, 16, 91174, 16, 10.

   CHIP TO BOARD CONDUCTORS

      PIN + AIR
      GEN 540, 4, 1, 91019, 16, 1019, 16, 0.0033
      GEN 544, 4, 1, 91019, 16, 1020, 16, 0.0033

      GEN 548, 2, 1, 91089, 16, 1089, 16, 0.00661
      GEN 550, 2, 1, 91090, 16, 1090, 16, 0.00661
```

```
GEN 552, 2, 1, 91108, 16, 1108, 16, 0.0033
GEN 554, 2, 1, 91109, 16, 1109, 16, 0.0033

GEN 556, 3, 1, 91182, 16, 1182, 16, 0.00661
GEN 559, 3, 1, 91183, 16, 1183, 16, 0.00661

GEN 562, 5, 1, 91154, 16, 1154, 16, 0.00661
GEN 567, 2, 1, 91155, 64, 1155, 64, 0.00661
GEN 569, 2, 1, 91156, 64, 1156, 64, 0.00661
GEN 571, 2, 1, 91157, 64, 1157, 64, 0.00661
GEN 573, 5, 1, 91158, 16, 1158, 16, 0.00661

GEN 578,14, 1, 91031, 16, 1031, 16, 0.00299  $ CONDUCTION THROUGH PC104 CONN
GEN 593, 9, 1, 91080, 16, 1080, 16, 0.00299  $ CONDUCTION THROUGH PC104 CONN

AIR
GEN 6010, 3, 1, 91171, 1, 1171, 1, 0.00505
GEN 6040, 3, 1, 91187, 1, 1187, 1, 0.00505
GEN 6070, 3, 1, 91203, 1, 1203, 1, 0.00505


********** I/O **********
  BOARD X-DIRECTION

GEN  603, 15, 1, 2001, 1, 2002, 1, 0.0098
GEN  618, 15, 1, 2017, 1, 2018, 1, 0.0098
GEN  633, 15, 1, 2033, 1, 2034, 1, 0.0098
GEN  648, 15, 1, 2049, 1, 2050, 1, 0.0098
GEN  663, 15, 1, 2065, 1, 2066, 1, 0.0098
GEN  678, 15, 1, 2081, 1, 2082, 1, 0.0098
GEN  693, 15, 1, 2097, 1, 2098, 1, 0.0098
GEN  708, 15, 1, 2113, 1, 2114, 1, 0.0098
GEN  723, 15, 1, 2129, 1, 2130, 1, 0.0098
GEN  738, 15, 1, 2145, 1, 2146, 1, 0.0098
GEN  753, 15, 1, 2161, 1, 2162, 1, 0.0098
GEN  768, 15, 1, 2177, 1, 2178, 1, 0.0098
GEN  783, 15, 1, 2193, 1, 2194, 1, 0.0098
GEN  798, 15, 1, 2209, 1, 2210, 1, 0.0098
GEN  813, 15, 1, 2225, 1, 2226, 1, 0.0098

  BOARD Y-DIRECTION

GEN  901, 14, 1, 2001, 1, 2017, 1, 0.0098
GEN  915, 14, 1, 2017, 1, 2033, 1, 0.0098
GEN  929, 14, 1, 2033, 1, 2049, 1, 0.0098
GEN  943, 14, 1, 2049, 1, 2065, 1, 0.0098
GEN  957, 14, 1, 2065, 1, 2081, 1, 0.0098
GEN  971, 14, 1, 2081, 1, 2097, 1, 0.0098
GEN  985, 14, 1, 2097, 1, 2113, 1, 0.0098
GEN  999, 14, 1, 2113, 1, 2129, 1, 0.0098
GEN 1013, 14, 1, 2129, 1, 2145, 1, 0.0098
GEN 1027, 14, 1, 2145, 1, 2161, 1, 0.0098
GEN 1041, 14, 1, 2161, 1, 2177, 1, 0.0098
GEN 1055, 14, 1, 2177, 1, 2193, 1, 0.0098
GEN 1069, 14, 1, 2193, 1, 2209, 1, 0.0098
GEN 1083, 14, 1, 2209, 1, 2225, 1, 0.0098

C
C   CHIP X-DIRECTION
C

GEN 1100, 5, 1, 92077, 16, 92078, 16, 10.
```

```
CHIP Y-DIRECTION

    GEN 1105, 4, 1, 92077, 16, 92093, 16, 10.
    GEN 1109, 4, 1, 92078, 16, 92094, 16, 10.

CHIP TO BOARD CONNECTORS

    PIN + AIR
    GEN 1120, 5, 1, 92077, 16, 2077, 16, 0.0033
    GEN 1125, 5, 1, 92078, 16, 2078, 16, 0.0033

    GEN 1130,14, 1, 92031, 16, 2031, 16, 0.00299  $ CONDUCTION THROUGH PC104 CONN
    GEN 1145, 9, 1, 92080, 16, 2080, 16, 0.00299  $ CONDUCTION THROUGH PC104 CONN


************************* VGA ************************
    BOARD X-DIRECTION

    GEN 1201, 15, 1, 3001, 1, 3002, 1, 0.0123
    GEN 1216, 15, 1, 3017, 1, 3018, 1, 0.0123
    GEN 1231, 15, 1, 3033, 1, 3034, 1, 0.0123
    GEN 1246, 15, 1, 3049, 1, 3050, 1, 0.0123
    GEN 1261, 15, 1, 3065, 1, 3066, 1, 0.0123
    GEN 1276, 15, 1, 3081, 1, 3082, 1, 0.0123
    GEN 1291, 15, 1, 3097, 1, 3098, 1, 0.0123
    GEN 1306, 15, 1, 3113, 1, 3114, 1, 0.0123
    GEN 1321, 15, 1, 3129, 1, 3130, 1, 0.0123
    GEN 1336, 15, 1, 3145, 1, 3146, 1, 0.0123
    GEN 1351, 15, 1, 3161, 1, 3162, 1, 0.0123
    GEN 1366, 15, 1, 3177, 1, 3178, 1, 0.0123
    GEN 1381, 15, 1, 3193, 1, 3194, 1, 0.0123
    GEN 1396, 15, 1, 3209, 1, 3210, 1, 0.0123
    GEN 1411, 15, 1, 3225, 1, 3226, 1, 0.0123

    BOARD Y-DIRECTION

    GEN 1501, 14, 1, 3001, 1, 3017, 1, 0.0123
    GEN 1515, 14, 1, 3017, 1, 3033, 1, 0.0123
    GEN 1529, 14, 1, 3033, 1, 3049, 1, 0.0123
    GEN 1543, 14, 1, 3049, 1, 3065, 1, 0.0123
    GEN 1557, 14, 1, 3065, 1, 3081, 1, 0.0123
    GEN 1571, 14, 1, 3081, 1, 3097, 1, 0.0123
    GEN 1585, 14, 1, 3097, 1, 3113, 1, 0.0123
    GEN 1599, 14, 1, 3113, 1, 3129, 1, 0.0123
    GEN 1613, 14, 1, 3129, 1, 3145, 1, 0.0123
    GEN 1627, 14, 1, 3145, 1, 3161, 1, 0.0123
    GEN 1641, 14, 1, 3161, 1, 3177, 1, 0.0123
    GEN 1655, 14, 1, 3177, 1, 3193, 1, 0.0123
    GEN 1669, 14, 1, 3193, 1, 3209, 1, 0.0123
    GEN 1683, 14, 1, 3209, 1, 3225, 1, 0.0123

CHIP X-DIRECTION

    GEN 1700, 4, 1, 93083, 1, 93084, 1, 10.
    GEN 1704, 4, 1, 93099, 1, 93100, 1, 10.
    GEN 1708, 4, 1, 93115, 1, 93116, 1, 10.
    GEN 1712, 4, 1, 93131, 1, 93132, 1, 10.
    GEN 1716, 4, 1, 93147, 1, 93148, 1, 10.
```

```
      GEN 17000, 4, 1, 93169, 1, 93170, 1, 10.
      GEN 17040, 4, 1, 93185, 1, 93186, 1, 10.

   CHIP Y-DIRECTION

      GEN 1720, 4, 1, 93083, 16, 93099, 16, 10.
      GEN 1724, 4, 1, 93084, 16, 93100, 16, 10.
      GEN 1728, 4, 1, 93085, 16, 93101, 16, 10.
      GEN 1732, 4, 1, 93086, 16, 93102, 16, 10.
      GEN 1736, 4, 1, 93087, 16, 93103, 16, 10.

      GEN 17200, 1, 1, 93169, 16, 93185, 16, 10.
      GEN 17240, 1, 1, 93170, 16, 93186, 16, 10.
      GEN 17280, 1, 1, 93171, 16, 93187, 16, 10.
      GEN 17320, 1, 1, 93172, 16, 93188, 16, 10.
      GEN 17360, 1, 1, 93173, 16, 93189, 16, 10.

   CHIP TO BOARD CONNECTORS

      PIN + AIR
      GEN 1740, 5, 1, 93083, 16, 3083, 16, 0.00661
      GEN 1745, 5, 1, 93087, 16, 3087, 16, 0.00661
      GEN 1750, 4, 1, 93084,  1, 3084,  1, 0.00661
      GEN 1754, 4, 1, 93148,  1, 3149,  1, 0.00661

      GEN 1758, 5, 1, 93169,  1, 3169,  1, 0.0033
      GEN 1763, 5, 1, 93185,  1, 3185,  1, 0.0033

      GEN 1768, 14, 1, 93031, 16, 3031, 16, 0.00299  $ CONDUCTION THROUGH PC104 CONN
      GEN 1782,  9, 1, 93080, 16, 3080, 16, 0.00299  $ CONDUCTION THROUGH PC104 CONN

      AIR
      GEN 1800, 3, 1, 93100, 1, 3100, 1, 0.00505
      GEN 1803, 3, 1, 93116, 1, 3116, 1, 0.00505
      GEN 1806, 3, 1, 93132, 1, 3132, 1, 0.00505

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

      CONVECTIVE CONDUCTORS

          THE FORCED CONVECTION CONDUCTOR VALUES ARE ARBITRARY, THE REAL
          CONDUCTOR VALUES ARE DETERMINED IN VARIABLES 1.

********** CPU PCB, TOP**********
      GEN 2000, 16, 1, 1001, 1, 8881, 0, 1.

      GEN 2020,  2, 1, 1017, 1, 8881, 0, 1.
      GEN 2022,  1, 1,91019, 1, 8881, 0, 2.$ 2. ETC USED TO ACCT FOR SIDE AREA OF CHIP
      GEN 2023, 11, 1, 1020, 1, 8881, 0, 1.
      GEN 2034,  1, 1,91031, 1, 8881, 0, 1.
      GEN 2035,  1, 1, 1032, 1, 8881, 0, 1.

      GEN 2040,  2, 1, 1033, 1, 8881, 0, 1.
      GEN 2042,  1, 1,91035, 1, 8881, 0, 2.
      GEN 2043, 11, 1, 1036, 1, 8881, 0, 1.
      GEN 2054,  1, 1,91047, 1, 8881, 0, 1.
      GEN 2055,  1, 1, 1048, 1, 8881, 0, 1.

      GEN 2060,  2, 1, 1049, 1, 8881, 0, 1.
      GEN 2062,  1, 1,91051, 1, 8881, 0, 2.
```

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GEN 2063, 11, 1, 1052, 1, 8881, 0, 1.
GEN 2074,  1, 1,91063, 1, 8881, 0, 1.
GEN 2075,  1, 1, 1064, 1, 8881, 0, 1.

GEN 2080, 2,  1, 1065, 1, 8881, 0, 1.
GEN 2082, 1,  1,91067, 1, 8881, 0, 2.
GEN 2083, 11, 1, 1068, 1, 8881, 0, 1.
GEN 2094, 2, 1, 91079, 1, 8881, 0, 1.

GEN 2100, 2,  1, 1081, 1, 8881, 0, 1.
    2101,       91083,    8881,    2.
GEN 2102, 5,  1, 1084, 1, 8881, 0, 1.
    2108,       91089,    8881,    2.
    2109,       91090,    8881,    2.
    2110,        1091,    8881,    1.
    2111,        1092,    8881,    1.
    2112,        1093,    8881,    1.
    2113,        1094,    8881,    1.
GEN 2114, 2, 1, 91095, 1, 8881, 0, 1.

GEN 2120, 8, 1,  1097, 1, 8881, 0, 1.
    2128,       91105,    8881,    2.
    2129,       91106,    8881,    2.
    2130,        1107,    8881,    1.
    2131,       91108,    8881,    2.
    2132,       91109,    8881,    2.
    2133,        1110,    8881,    1.
    2134,       91111,    8881,    1.
    2135,       91112,    8881,    1.

GEN 2140, 11, 1, 1113, 1, 8881, 0, 1.
GEN 2150,  2, 1,91124, 1, 8881, 0, 2.
    2153,        1126,    8881,    1.
    2154,       91127,    8881,    1.
    2155,       91128,    8881,    1.

GEN 2160,  8, 1, 1129, 1, 8881, 0, 1.
GEN 2168,  6, 1, 1137, 1, 8881, 0, 1.
    2174,       91143,    8881,    1.
    2175,       91144,    8881,    1.

GEN 2180,  9, 1, 1145, 1, 8881, 0, 1.
GEN 2188,  5, 1,91154, 1, 8881, 0, 1.7
    2194,       91159,    8881,    1.
    2195,       91160,    8881,    1.

GEN 2200,  9, 1, 1161, 1, 8881, 0, 1.
GEN 2208,  5, 1,91170, 1, 8881, 0, 1.2
    2214,       91175,    8881,    1.
    2215,       91176,    8881,    1.

GEN  2220,  5, 1, 1177, 1, 8881, 0, 1.
GEN  2225,  2, 1,91182, 1, 8881, 0, 2.
     2227,        1184,    8881,    1.
     2228,        1185,    8881,    1.
GEN  2229,  5, 1,91186, 1, 8881, 0, 1.2
GEN  2234,  2, 1,91191, 1, 8881, 0, 1.

GEN  2240,  5, 1, 1193, 1, 8881, 0, 1.
GEN  2245,  2, 1,91198, 1, 8881, 0, 1.5
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          2247,         1200,    8881,    1.
          2248,         1201,    8881,    1.
GEN  2249,  5, 1,91202, 1, 8881, 0, 1.2
GEN  2254,  2, 1, 1207, 1, 8881, 0, 1.

GEN  2260,  5, 1, 1209, 1, 8881, 0, 1.
GEN  2265,  2, 1,91214, 1, 8881, 0, 2.
GEN  2267,  2, 1, 1216, 1, 8881, 0, 1.
GEN  2269,  5, 1,91218, 1, 8881, 0, 1.7
GEN  2274,  1, 1,91223, 1, 8881, 0, 1.
GEN  2275,  1, 1, 1224, 1, 8881, 0, 1.

GEN  2280, 16, 1, 1225, 1, 8881, 0, 1.

          CPU PCB, BOTTOM
          CONDUCTION THROUGH AIR TO MIDDLE BOARD
AC    1.
      GEN 2300, 16, 1, 1001, 1, 7771, 0, 5.66E-05
      GEN 2320, 16, 1, 1017, 1, 7771, 0, 5.66E-05
      GEN 2340, 16, 1, 1033, 1, 7771, 0, 5.66E-05
      GEN 2360, 16, 1, 1049, 1, 7771, 0, 5.66E-05
      GEN 2380, 16, 1, 1065, 1, 7771, 0, 5.66E-05
      GEN 2400, 16, 1, 1081, 1, 7771, 0, 5.66E-05
      GEN 2420, 16, 1, 1097, 1, 7771, 0, 5.66E-05
      GEN 2440, 16, 1, 1113, 1, 7771, 0, 5.66E-05
      GEN 2460, 16, 1, 1129, 1, 7771, 0, 5.66E-05
      GEN 2480, 16, 1, 1145, 1, 7771, 0, 5.66E-05
      GEN 2500, 16, 1, 1161, 1, 7771, 0, 5.66E-05
      GEN 2520, 16, 1, 1177, 1, 7771, 0, 5.66E-05
      GEN 2540, 16, 1, 1193, 1, 7771, 0, 5.66E-05
      GEN 2560, 16, 1, 1209, 1, 7771, 0, 5.66E-05
      GEN 2580, 16, 1, 1225, 1, 7771, 0, 5.66E-05

AC    1.

********** I/O PCB, TOP **********

      GEN 2600, 16, 1, 2001, 1, 8882, 0, 1.

      GEN 2620, 14, 1, 2017, 1, 8882, 0, 1.
      GEN 2634,  1, 1,92031, 1, 8882, 0, 1.
      GEN 2635,  1, 1, 2032, 1, 8882, 0, 1.

      GEN 2640, 14, 1, 2033, 1, 8882, 0, 1.
      GEN 2654,  1, 1,92047, 1, 8882, 0, 1.
      GEN 2655,  1, 1, 2048, 1, 8882, 0, 1.

      GEN 2660, 14, 1, 2049, 1, 8882, 0, 1.
      GEN 2674,  1, 1,92063, 1, 8882, 0, 1.
      GEN 2675,  1, 1, 2064, 1, 8882, 0, 1.

      GEN 2680, 12, 1,  2065, 1, 8882, 0, 1.
      GEN 2692,  2, 1, 92077, 1, 8882, 0, 2.
      GEN 2694,  1, 1, 92079, 1, 8882, 0, 1.
      GEN 2695,  1, 1, 92080, 1, 8882, 0, 1.

      GEN 2700, 12, 1,  2081, 1, 8882, 0, 1.
      GEN 2712,  2, 1, 92093, 1, 8882, 0, 1.5
      GEN 2714,  1, 1, 92095, 1, 8882, 0, 1.
      GEN 2715,  1, 1, 92096, 1, 8882, 0, 1.
```

```
GEN 2720, 12, 1,  2097, 1, 8882, 0, 1.
GEN 2732,  2, 1, 92109, 1, 8882, 0, 1.5
GEN 2734,  1, 1, 92111, 1, 8882, 0, 1.
GEN 2735,  1, 1, 92112, 1, 8882, 0, 1.

GEN 2740, 12, 1,  2113, 1, 8882, 0, 1.
GEN 2752,  2, 1, 92125, 1, 8882, 0, 1.5
GEN 2754,  1, 1, 92127, 1, 8882, 0, 1.
GEN 2755,  1, 1, 92128, 1, 8882, 0, 1.

GEN 2760, 12, 1,  2129, 1, 8882, 0, 1.
GEN 2772,  2, 1, 92141, 1, 8882, 0, 2.
GEN 2774,  1, 1, 92143, 1, 8882, 0, 1.
GEN 2775,  1, 1, 92144, 1, 8882, 0, 1.

GEN 2780, 14, 1, 2145, 1, 8882, 0, 1.
GEN 2794,  2, 1,92159, 1, 8882, 0, 1.

GEN 2800, 14, 1, 2161, 1, 8882, 0, 1.
GEN 2814,  2, 1,92175, 1, 8882, 0, 1.

GEN 2820, 14, 1, 2177, 1, 8882, 0, 1.
GEN 2834,  2, 1,92191, 1, 8882, 0, 1.

GEN 2840, 14, 1, 2193, 1, 8882, 0, 1.
GEN 2854,  2, 1,92207, 1, 8882, 0, 1.

GEN 2860, 14, 1, 2209, 1, 8882, 0, 1.
GEN 2874,  1, 1,92223, 1, 8882, 0, 1.
GEN 2875,  1, 1, 2224, 1, 8882, 0, 1.

GEN 2880, 14, 1, 2225, 1, 8882, 0, 1.
GEN 2894,  1, 1,92239, 1, 8882, 0, 1.
GEN 2895,  1, 1, 2240, 1, 8882, 0, 1.

;          I/O PCB, BOTTOM
;AC    1.
      GEN 2900, 16, 1, 2001, 1, 7772, 0, 5.66E-05
      GEN 2920, 16, 1, 2017, 1, 7772, 0, 5.66E-05
      GEN 2940, 16, 1, 2033, 1, 7772, 0, 5.66E-05
      GEN 2960, 16, 1, 2049, 1, 7772, 0, 5.66E-05
      GEN 2980, 16, 1, 2065, 1, 7772, 0, 5.66E-05
      GEN 3000, 16, 1, 2081, 1, 7772, 0, 5.66E-05
      GEN 3020, 16, 1, 2097, 1, 7772, 0, 5.66E-05
      GEN 3040, 16, 1, 2113, 1, 7772, 0, 5.66E-05
      GEN 3060, 16, 1, 2129, 1, 7772, 0, 5.66E-05
      GEN 3080, 16, 1, 2145, 1, 7772, 0, 5.66E-05
      GEN 3100, 16, 1, 2161, 1, 7772, 0, 5.66E-05
      GEN 3120, 16, 1, 2177, 1, 7772, 0, 5.66E-05
      GEN 3140, 16, 1, 2193, 1, 7772, 0, 5.66E-05
      GEN 3160, 16, 1, 2209, 1, 7772, 0, 5.66E-05
      GEN 3180, 16, 1, 2225, 1, 7772, 0, 5.66E-05
;FAC    1.
;
;
;********************** VGA PCB, TOP ***************************
;
      GEN 3200, 16, 1, 3001, 1, 8883, 0, 1.
;
```

```
GEN 3220, 14, 1,  3017, 1, 8883, 0, 1.
GEN 3234,  1, 1, 93031, 1, 8883, 0, 1.
GEN 3235,  1, 1,  3032, 1, 8883, 0, 1.

GEN 3240, 14, 1, 3033, 1, 8883, 0, 1.
GEN 3254,  1, 1,93047, 1, 8883, 0, 1.
GEN 3255,  1, 1, 3048, 1, 8883, 0, 1.

GEN 3260, 14, 1, 3049, 1, 8883, 0, 1.
GEN 3274,  1, 1,93063, 1, 8883, 0, 1.
GEN 3275,  1, 1, 3064, 1, 8883, 0, 1.

GEN 3280, 14, 1, 3065, 1, 8883, 0, 1.
GEN 3294,  2, 1,93079, 1, 8883, 0, 1.

GEN 3300,  2, 1,  3081, 1, 8883, 0, 1.
GEN 3302,  5, 1, 93083, 1, 8883, 0, 1.7
GEN 3307,  7, 1,  3088, 1, 8883, 0, 1.
GEN 3314,  2, 1, 93095, 1, 8883, 0, 1.

GEN 3320,  2, 1,  3097, 1, 8883, 0, 1.
GEN 3322,  5, 1, 93099, 1, 8883, 0, 1.2
GEN 3327,  7, 1,  3104, 1, 8883, 0, 1.
GEN 3334,  2, 1, 93111, 1, 8883, 0, 1.

GEN 3340,  2, 1,  3113, 1, 8883, 0, 1.
GEN 3342,  5, 1, 93115, 1, 8883, 0, 1.2
GEN 3347,  7, 1,  3120, 1, 8883, 0, 1.
GEN 3354,  2, 1, 93127, 1, 8883, 0, 1.

GEN 3360,  2, 1,  3129, 1, 8883, 0, 1.
GEN 3362,  5, 1, 93131, 1, 8883, 0, 1.2
GEN 3367,  7, 1,  3136, 1, 8883, 0, 1.
GEN 3374,  2, 1, 93143, 1, 8883, 0, 1.

GEN 3380,  2, 1,  3145, 1, 8883, 0, 1.
GEN 3382,  5, 1, 93147, 1, 8883, 0, 1.7
GEN 3387,  7, 1,  3152, 1, 8883, 0, 1.
GEN 3394,  2, 1, 93159, 1, 8883, 0, 1.

GEN 3400,  8, 1,  3161, 1, 8883, 0, 1.
GEN 3408,  5, 1, 93169, 1, 8883, 0, 1.7
GEN 3413,  1, 1,  3174, 1, 8883, 0, 1.
GEN 3414,  2, 1, 93175, 1, 8883, 0, 1.

GEN 3420,  8, 1,  3177, 1, 8883, 0, 1.
GEN 3428,  5, 1, 93185, 1, 8883, 0, 1.7
GEN 3433,  1, 1,  3190, 1, 8883, 0, 1.
GEN 3434,  2, 1, 93191, 1, 8883, 0, 1.

GEN 3440, 14, 1, 3193, 1, 8883, 0, 1.
GEN 3454,  2, 1,93207, 1, 8883, 0, 1.

GEN 3460, 14, 1, 3209, 1, 8883, 0, 1.
GEN 3474,  1, 1,93223, 1, 8883, 0, 1.
GEN 3475,  1, 1, 3224, 1, 8883, 0, 1.

GEN 3480, 14, 1, 3225, 1, 8883, 0, 1.
GEN 3494,  1, 1,93239, 1, 8883, 0, 1.
GEN 3495,  1, 1, 3240, 1, 8883, 0, 1.
```

```
          VGA PCB, BOTTOM
AC     1.
       GEN 3500, 16, 1, 3001, 1, 7773, 0, 5.66E-05
       GEN 3520, 16, 1, 3017, 1, 7773, 0, 5.66E-05
       GEN 3540, 16, 1, 3033, 1, 7773, 0, 5.66E-05
       GEN 3560, 16, 1, 3049, 1, 7773, 0, 5.66E-05
       GEN 3580, 16, 1, 3065, 1, 7773, 0, 5.66E-05
       GEN 3600, 16, 1, 3081, 1, 7773, 0, 5.66E-05
       GEN 3620, 16, 1, 3097, 1, 7773, 0, 5.66E-05
       GEN 3640, 16, 1, 3113, 1, 7773, 0, 5.66E-05
       GEN 3660, 16, 1, 3129, 1, 7773, 0, 5.66E-05
       GEN 3680, 16, 1, 3145, 1, 7773, 0, 5.66E-05
       GEN 3700, 16, 1, 3161, 1, 7773, 0, 5.66E-05
       GEN 3720, 16, 1, 3177, 1, 7773, 0, 5.66E-05
       GEN 3740, 16, 1, 3193, 1, 7773, 0, 5.66E-05
       GEN 3760, 16, 1, 3209, 1, 7773, 0, 5.66E-05
       GEN 3780, 16, 1, 3225, 1, 7773, 0, 5.66E-05

AC     1.

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

   RADIATION CONDUCTORS

********** CPU **********

  FAC CARD USED TO INCREASE EMISS TO 0.85 FROM EMISS = 0.80
  AND FAC CARD USED TO ACCT FOR AREA AUGMENTATION DUE TO SIDES OF CHIPS
FAC     1.062
AC      1.3
  FAC = 1.3 = 1.062 (CONVERTS EMISS) * 1.22 (COMPENSATES FOR AVERAGE EFFECT
  OF SIDE AREA OF CHIPS)

       GEN -4000, 16, 1, 1001, 1, 9999, 0, 2.875E-05

       GEN -4020,  2, 1, 1017, 1, 9999, 0, 2.875E-05
       GEN -4022,  1, 1,91019, 1, 9999, 0, 2.875E-05
       GEN -4023, 11, 1, 1020, 1, 9999, 0, 2.875E-05
       GEN -4034,  1, 1,91031, 1, 9999, 0, 2.875E-05
       GEN -4035,  1, 1, 1032, 1, 9999, 0, 2.875E-05

       GEN -4040,  2, 1, 1033, 1, 9999, 0, 2.875E-05
       GEN -4042,  1, 1,91035, 1, 9999, 0, 2.875E-05
       GEN -4043, 11, 1, 1036, 1, 9999, 0, 2.875E-05
       GEN -4054,  1, 1,91047, 1, 9999, 0, 2.875E-05
       GEN -4055,  1, 1, 1048, 1, 9999, 0, 2.875E-05

       GEN -4060,  2, 1, 1049, 1, 9999, 0, 2.875E-05
       GEN -4062,  1, 1,91051, 1, 9999, 0, 2.875E-05
       GEN -4063, 11, 1, 1052, 1, 9999, 0, 2.875E-05
       GEN -4074,  1, 1,91063, 1, 9999, 0, 2.875E-05
       GEN -4075,  1, 1, 1064, 1, 9999, 0, 2.875E-05

       GEN -4080, 2,  1, 1065, 1, 9999, 0, 2.875E-05
       GEN -4082, 1,  1,91067, 1, 9999, 0, 2.875E-05
       GEN -4083, 11, 1, 1068, 1, 9999, 0, 2.875E-05
       GEN -4094, 2, 1, 91079, 1, 9999, 0, 2.875E-05

       GEN -4100, 2,  1, 1081, 1, 9999, 0, 2.875E-05
```

```
    -4101,        91083,    9999,    2.875E-05
GEN -4102, 5,  1, 1084, 1, 9999, 0, 2.875E-05
    -4108,        91089,    9999,    2.875E-05
    -4109,        91090,    9999,    2.875E-05
    -4110,         1091,    9999,    2.875E-05
    -4111,         1092,    9999,    2.875E-05
    -4112,         1093,    9999,    2.875E-05
    -4113,         1094,    9999,    2.875E-05
GEN -4114, 2, 1, 91095, 1, 9999, 0, 2.875E-05

GEN -4120, 8, 1,  1097, 1, 9999, 0, 2.875E-05
    -4128,        91105,    9999,    2.875E-05
    -4129,        91106,    9999,    2.875E-05
    -4130,         1107,    9999,    2.875E-05
    -4131,        91108,    9999,    2.875E-05
    -4132,        91109,    9999,    2.875E-05
    -4133,         1110,    9999,    2.875E-05
    -4134,        91111,    9999,    2.875E-05
    -4135,        91112,    9999,    2.875E-05

GEN -4140, 11, 1, 1113, 1, 9999, 0, 2.875E-05
GEN -4150,  2, 1,91124, 1, 9999, 0, 2.875E-05
    -4153,         1126,    9999,    2.875E-05
    -4154,        91127,    9999,    2.875E-05
    -4155,        91128,    9999,    2.875E-05

GEN -4160,  8, 1, 1129, 1, 9999, 0, 2.875E-05
GEN -4168,  6, 1, 1137, 1, 9999, 0, 2.875E-05
    -4174,        91143,    9999,    2.875E-05
    -4175,        91144,    9999,    2.875E-05

GEN -4180,  9, 1, 1145, 1, 9999, 0, 2.875E-05
GEN -4188,  5, 1,91154, 1, 9999, 0, 2.875E-05
    -4194,        91159,    9999,    2.875E-05
    -4195,        91160,    9999,    2.875E-05

GEN  -4200,  9, 1, 1161, 1, 9999, 0, 2.875E-05
GEN  -4208,  5, 1,91170, 1, 9999, 0, 2.875E-05
     -4214,        91175,    9999,    2.875E-05
     -4215,        91176,    9999,    2.875E-05

GEN  -4220,  5, 1, 1177, 1, 9999, 0, 2.875E-05
GEN  -4225,  2, 1,91182, 1, 9999, 0, 2.875E-05
     -4227,         1184,    9999,    2.875E-05
     -4228,         1185,    9999,    2.875E-05
GEN  -4229,  5, 1,91186, 1, 9999, 0, 2.875E-05
GEN  -4234,  2, 1,91191, 1, 9999, 0, 2.875E-05

GEN  -4240,  5, 1, 1193, 1, 9999, 0, 2.875E-05
GEN  -4245,  2, 1,91198, 1, 9999, 0, 2.875E-05
     -4247,         1200,    9999,    2.875E-05
     -4248,         1201,    9999,    2.875E-05
GEN  -4249,  5, 1, 1201, 1, 9999, 0, 2.875E-05
GEN  -4254,  2, 1, 1207, 1, 9999, 0, 2.875E-05

GEN  -4260,  5, 1, 1209, 1, 9999, 0, 2.875E-05
GEN  -4265,  2, 1,91214, 1, 9999, 0, 2.875E-05
GEN  -4267,  2, 1, 1216, 1, 9999, 0, 2.875E-05
GEN  -4269,  5, 1,91218, 1, 9999, 0, 2.875E-05
GEN  -4274,  1, 1,91223, 1, 9999, 0, 2.875E-05
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GEN  -4275,  1, 1, 1224, 1, 9999, 0, 2.875E-05

GEN  -4280, 16, 1, 1225, 1, 9999, 0, 2.875E-05

C   1.
**** ********************** I/O **********************************

C    1.15

GEN -4300, 16, 1, 2001, 1, 9999, 0, 2.875E-05

GEN -4320, 14, 1, 2017, 1, 9999, 0, 2.875E-05
GEN -4334,  1, 1,92031, 1, 9999, 0, 2.875E-05
GEN -4335,  1, 1, 2032, 1, 9999, 0, 2.875E-05

GEN -4340, 14, 1, 2033, 1, 9999, 0, 2.875E-05
GEN -4354,  1, 1,92047, 1, 9999, 0, 2.875E-05
GEN -4355,  1, 1, 2048, 1, 9999, 0, 2.875E-05

GEN -4360, 14, 1, 2049, 1, 9999, 0, 2.875E-05
GEN -4374,  1, 1,92063, 1, 9999, 0, 2.875E-05
GEN -4375,  1, 1, 2064, 1, 9999, 0, 2.875E-05

GEN -4380, 12, 1, 2065, 1, 9999, 0, 2.875E-05
GEN -4392,  2, 1, 92077, 1, 9999, 0, 2.875E-05
GEN -4394,  1, 1, 92079, 1, 9999, 0, 2.875E-05
GEN -4395,  1, 1, 92080, 1, 9999, 0, 2.875E-05

GEN -4400, 12, 1,  2081, 1, 9999, 0, 2.875E-05
GEN -4412,  2, 1, 92093, 1, 9999, 0, 2.875E-05
GEN -4414,  1, 1, 92095, 1, 9999, 0, 2.875E-05
GEN -4415,  1, 1, 92096, 1, 9999, 0, 2.875E-05

GEN -4420, 12, 1,  2097, 1, 9999, 0, 2.875E-05
GEN -4432,  2, 1, 92109, 1, 9999, 0, 2.875E-05
GEN -4433,  1, 1, 92111, 1, 9999, 0, 2.875E-05
GEN -4434,  1, 1, 92112, 1, 9999, 0, 2.875E-05

GEN -4440, 12, 1,  2113, 1, 9999, 0, 2.875E-05
GEN -4452,  2, 1, 92125, 1, 9999, 0, 2.875E-05
GEN -4454,  1, 1, 92127, 1, 9999, 0, 2.875E-05
GEN -4455,  1, 1, 92128, 1, 9999, 0, 2.875E-05

GEN -4460, 12, 1,  2129, 1, 9999, 0, 2.875E-05
GEN -4472,  2, 1, 92141, 1, 9999, 0, 2.875E-05
GEN -4474,  1, 1, 92143, 1, 9999, 0, 2.875E-05
GEN -4475,  1, 1, 92144, 1, 9999, 0, 2.875E-05

GEN -4480, 14, 1, 2145, 1, 9999, 0, 2.875E-05
GEN -4494,  2, 1,92159, 1, 9999, 0, 2.875E-05

GEN -4500, 14, 1, 2161, 1, 9999, 0, 2.875E-05
GEN -4514,  2, 1,92175, 1, 9999, 0, 2.875E-05

GEN -4520, 14, 1, 2177, 1, 9999, 0, 2.875E-05
GEN -4534,  2, 1,92191, 1, 9999, 0, 2.875E-05

GEN -4540, 14, 1, 2193, 1, 9999, 0, 2.875E-05
GEN -4554,  2, 1,92207, 1, 9999, 0, 2.875E-05
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GEN -4560, 14, 1, 2209, 1, 9999, 0, 2.875E-05
GEN -4574,  1, 1,92223, 1, 9999, 0, 2.875E-05
GEN -4575,  1, 1, 2224, 1, 9999, 0, 2.875E-05

GEN -4580, 14, 1, 2225, 1, 9999, 0, 2.875E-05
GEN -4594,  1, 1,92239, 1, 9999, 0, 2.875E-05
GEN -4595,  1, 1, 2240, 1, 9999, 0, 2.875E-05

AC    1.
********************************* VGA ***********************************

AC    1.06
GEN -4600, 16, 1, 3001, 1, 9999, 0, 2.875E-05

GEN -4620, 14, 1,  3017, 1, 9999, 0, 2.875E-05
GEN -4634,  1, 1, 93031, 1, 9999, 0, 2.875E-05
GEN -4635,  1, 1,  3032, 1, 9999, 0, 2.875E-05

GEN -4640, 14, 1, 3033, 1, 9999, 0, 2.875E-05
GEN -4654,  1, 1,93047, 1, 9999, 0, 2.875E-05
GEN -4655,  1, 1, 3048, 1, 9999, 0, 2.875E-05

GEN -4660, 14, 1, 3049, 1, 9999, 0, 2.875E-05
GEN -4674,  1, 1,93063, 1, 9999, 0, 2.875E-05
GEN -4675,  1, 1, 3064, 1, 9999, 0, 2.875E-05

GEN -4680, 14, 1, 3065, 1, 9999, 0, 2.875E-05
GEN -4694,  2, 1,93079, 1, 9999, 0, 2.875E-05

GEN -4700,  2, 1,  3081, 1, 9999, 0, 2.875E-05
GEN -4702,  5, 1, 93083, 1, 9999, 0, 2.875E-05
GEN -4707,  7, 1,  3088, 1, 9999, 0, 2.875E-05
GEN -4714,  2, 1, 93095, 1, 9999, 0, 2.875E-05

GEN -4720,  2, 1,  3097, 1, 9999, 0, 2.875E-05
GEN -4722,  5, 1, 93099, 1, 9999, 0, 2.875E-05
GEN -4727,  7, 1,  3104, 1, 9999, 0, 2.875E-05
GEN -4734,  2, 1, 93111, 1, 9999, 0, 2.875E-05

GEN -4740,  2, 1,  3113, 1, 9999, 0, 2.875E-05
GEN -4742,  5, 1, 93115, 1, 9999, 0, 2.875E-05
GEN -4747,  7, 1,  3120, 1, 9999, 0, 2.875E-05
GEN -4754,  2, 1, 93127, 1, 9999, 0, 2.875E-05

GEN -4760,  2, 1,  3129, 1, 9999, 0, 2.875E-05
GEN -4762,  5, 1, 93131, 1, 9999, 0, 2.875E-05
GEN -4767,  7, 1,  3136, 1, 9999, 0, 2.875E-05
GEN -4774,  2, 1, 93143, 1, 9999, 0, 2.875E-05

GEN -4780,  2, 1,  3145, 1, 9999, 0, 2.875E-05
GEN -4782,  5, 1, 93147, 1, 9999, 0, 2.875E-05
GEN -4787,  7, 1,  3152, 1, 9999, 0, 2.875E-05
GEN -4794,  2, 1, 93159, 1, 9999, 0, 2.875E-05

GEN -4800,  8, 1, 3161, 1, 9999, 0, 2.875E-05
GEN -4808,  5, 1, 93169, 1, 9999, 0, 2.875E-05
GEN -4813,  1, 1, 3174, 1, 9999, 0, 2.875E-05
GEN -4814,  2, 1, 93175, 1, 9999, 0, 2.875E-05

GEN -4820,  8, 1, 3177, 1, 9999, 0, 2.875E-05
```

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      GEN -4828,  5, 1, 93185, 1, 9999, 0, 2.875E-05
      GEN -4833,  1, 1, 3190, 1, 9999, 0, 2.875E-05
      GEN -4834,  2, 1, 93191, 1, 9999, 0, 2.875E-05

      GEN -4840, 14, 1, 3193, 1, 9999, 0, 2.875E-05
      GEN -4854,  2, 1,93207, 1, 9999, 0, 2.875E-05

      GEN -4860, 14, 1, 3209, 1, 9999, 0, 2.875E-05
      GEN -4874,  1, 1,93223, 1, 9999, 0, 2.875E-05
      GEN -4875,  1, 1, 3224, 1, 9999, 0, 2.875E-05

      GEN -4880, 14, 1, 3225, 1, 9999, 0, 2.875E-05
      GEN -4894,  1, 1,93239, 1, 9999, 0, 2.875E-05
      GEN -4895,  1, 1, 3240, 1, 9999, 0, 2.875E-05
AC    1.

ADER VARIABLES 1, PCB

  CALCULATE CONVECTION CONDUCTORS

      VAIR = 4.17
      ANODE = 0.236*0.236*0.0254*0.0254

      CALCULATE HEAT TRANSFER COEFFICIENT AS FUNCTION OF DOWNSTREAM POSITION

      H = (0.3925*Pr^0.33*Re^0.5)*K/X
          WHERE Re = RHO*VAIR*X/DYN. VISCOSITY
          * OR / 0.0254 USED TO CONVERT FROM INCH TO METERS

      H1001=.3925*((.71**.333)*(1.14*VAIR*0.118*.0254/1.9E-05)**.5)*.027/.118
     &/0.0254
      H1002=.3925*((.71**.333)*(1.14*VAIR*0.354*.0254/1.9E-05)**.5)*.027/.354
     &/0.0254
      H1003=.3925*((.71**.333)*(1.14*VAIR*0.590*.0254/1.9E-05)**.5)*.027/.590
     &/0.0254
      H1004=.3925*((.71**.333)*(1.14*VAIR*0.826*.0254/1.9E-05)**.5)*.027/.826
     &/0.0254
      H1005=.3925*((.71**.333)*(1.14*VAIR*1.062*.0254/1.9E-05)**.5)*.027/1.062
     &/0.0254
      H1006=.3925*((.71**.333)*(1.14*VAIR*1.298*.0254/1.9E-05)**.5)*.027/1.298
     &/0.0254
      H1007=.3925*((.71**.333)*(1.14*VAIR*1.534*.0254/1.9E-05)**.5)*.027/1.534
     &/0.0254
      H1008=.3925*((.71**.333)*(1.14*VAIR*1.770*.0254/1.9E-05)**.5)*.027/1.770
     &/0.0254
      H1009=.3925*((.71**.333)*(1.14*VAIR*2.006*.0254/1.9E-05)**.5)*.027/2.006
     &/0.0254
      H1010=.3925*((.71**.333)*(1.14*VAIR*2.242*.0254/1.9E-05)**.5)*.027/2.242
     &/0.0254
      H1011=.3925*((.71**.333)*(1.14*VAIR*2.478*.0254/1.9E-05)**.5)*.027/2.478
     &/0.0254
      H1012=.3925*((.71**.333)*(1.14*VAIR*2.714*.0254/1.9E-05)**.5)*.027/2.714
     &/0.0254
      H1013=.3925*((.71**.333)*(1.14*VAIR*2.950*.0254/1.9E-05)**.5)*.027/2.950
     &/0.0254
      H1014=.3925*((.71**.333)*(1.14*VAIR*3.186*.0254/1.9E-05)**.5)*.027/3.186
     &/0.0254
      H1015=.3925*((.71**.333)*(1.14*VAIR*3.422*.0254/1.9E-05)**.5)*.027/3.422
     &/0.0254
C
```

```
LOGIC USED TO ACCT FOR SIDE AREA OF CHIPS

      SET ALL CONDUCTORS TO INITIAL VALUE OF 1 SO THAT ITERATIONS DO NOT
      CAUSE MISCALCULATION OF CONVECTION CONDUCTORS

************************** PROCESSOR ******************************
      DO 10 ITEST = 0, 15
      G(2000+ITEST) = 1.
      G(2020+ITEST) = 1.
      G(2040+ITEST) = 1.
      G(2060+ITEST) = 1.
      G(2080+ITEST) = 1.
      G(2100+ITEST) = 1.
      G(2120+ITEST) = 1.
      G(2140+ITEST) = 1.
      G(2160+ITEST) = 1.
      G(2180+ITEST) = 1.
      G(2200+ITEST) = 1.
      G(2220+ITEST) = 1.
      G(2240+ITEST) = 1.
      G(2260+ITEST) = 1.
      G(2280+ITEST) = 1.

************************** I/O ************************************************
      G(2600+ITEST) = 1.
      G(2620+ITEST) = 1.
      G(2640+ITEST) = 1.
      G(2660+ITEST) = 1.
      G(2680+ITEST) = 1.
      G(2700+ITEST) = 1.
      G(2720+ITEST) = 1.
      G(2740+ITEST) = 1.
      G(2760+ITEST) = 1.
      G(2780+ITEST) = 1.
      G(2800+ITEST) = 1.
      G(2820+ITEST) = 1.
      G(2840+ITEST) = 1.
      G(2860+ITEST) = 1.
      G(2880+ITEST) = 1.

************************** VGA ************************************************
      G(3200+ITEST) = 1.
      G(3220+ITEST) = 1.
      G(3240+ITEST) = 1.
      G(3260+ITEST) = 1.
      G(3280+ITEST) = 1.
      G(3300+ITEST) = 1.
      G(3320+ITEST) = 1.
      G(3340+ITEST) = 1.
      G(3360+ITEST) = 1.
      G(3380+ITEST) = 1.
      G(3400+ITEST) = 1.
      G(3420+ITEST) = 1.
      G(3440+ITEST) = 1.
      G(3460+ITEST) = 1.
      G(3480+ITEST) = 1.
F10   CONTINUE
C
C  ESTABLISH MULTIPLICATION FACTORS THAT ACCT FOR SIDE AREA OF CHIP
C    PROCESSOR BOARD
```

```
      G2022 = 2.

      G2042 = 2.

      G2062 = 2.

      G2082 = 2.

      G2101 = 2.
      G2108 = 2.
      G2109 = 2.

      G2128 = 2.
      G2129 = 2.
      G2131 = 2.
      G2132 = 2.

      G2150 = 2.
      G2151 = 2.

      G2188 = 1.7
      G2189 = 1.7
      G2190 = 1.7
      G2191 = 1.7
      G2192 = 1.7

      G2208 = 1.2
      G2209 = 1.2
      G2210 = 1.2
      G2211 = 1.2
      G2212 = 1.2

      G2225 = 2.
      G2226 = 2.
      G2229 = 1.2
      G2230 = 1.2
      G2231 = 1.2
      G2232 = 1.2
      G2233 = 1.2

      G2245 = 1.5
      G2246 = 1.5
      G2249 = 1.2
      G2250 = 1.2
      G2251 = 1.2
      G2252 = 1.2
      G2253 = 1.2

      G2265 = 2.
      G2266 = 2.
      G2269 = 1.7
      G2270 = 1.7
      G2271 = 1.7
      G2272 = 1.7
      G2273 = 1.7

C     I/O BOARD
      G2692 = 2.
      G2693 = 2.
```

```
      G2712 = 1.5
      G2713 = 1.5

      G2732 = 1.5
      G2733 = 1.5

      G2752 = 1.5
      G2753 = 1.5

      G2772 = 2.
      G2773 = 2.

    VGA BOARD
      G3302 = 1.7
      G3303 = 1.7
      G3304 = 1.7
      G3305 = 1.7
      G3306 = 1.7

      G3322 = 1.2
      G3323 = 1.2
      G3324 = 1.2
      G3325 = 1.2
      G3326 = 1.2

      G3342 = 1.2
      G3343 = 1.2
      G3344 = 1.2
      G3345 = 1.2
      G3346 = 1.2

      G3362 = 1.2
      G3363 = 1.2
      G3364 = 1.2
      G3365 = 1.2
      G3366 = 1.2

      G3382 = 1.7
      G3383 = 1.7
      G3384 = 1.7
      G3385 = 1.7
      G3386 = 1.7

      G3408 = 1.7
      G3409 = 1.7
      G3410 = 1.7
      G3411 = 1.7
      G3412 = 1.7

      G3428 = 1.7
      G3429 = 1.7
      G3430 = 1.7
      G3431 = 1.7
      G3432 = 1.7
C
C     CALCULATE CONVECTION COUPLINGS
C***************************** CPU ************************************************
F     DO 20 JTEST = 0, 15
      G(2000+JTEST) = G(2000+JTEST) * H1001 * ANODE
```

```
      G(2020+JTEST) = G(2020+JTEST) * H1002 * ANODE
      G(2040+JTEST) = G(2040+JTEST) * H1003 * ANODE
      G(2060+JTEST) = G(2060+JTEST) * H1004 * ANODE
      G(2080+JTEST) = G(2080+JTEST) * H1005 * ANODE
      G(2100+JTEST) = G(2100+JTEST) * H1006 * ANODE
      G(2120+JTEST) = G(2120+JTEST) * H1007 * ANODE
      G(2140+JTEST) = G(2140+JTEST) * H1008 * ANODE
      G(2160+JTEST) = G(2160+JTEST) * H1009 * ANODE
      G(2180+JTEST) = G(2180+JTEST) * H1010 * ANODE
      G(2200+JTEST) = G(2200+JTEST) * H1011 * ANODE
      G(2220+JTEST) = G(2220+JTEST) * H1012 * ANODE
      G(2240+JTEST) = G(2240+JTEST) * H1013 * ANODE
      G(2260+JTEST) = G(2260+JTEST) * H1014 * ANODE
      G(2280+JTEST) = G(2280+JTEST) * H1015 * ANODE

 ***************************** I/O ***********************************************
      G(2600+JTEST) = G(2600+JTEST) * H1001 * ANODE
      G(2620+JTEST) = G(2620+JTEST) * H1002 * ANODE
      G(2640+JTEST) = G(2640+JTEST) * H1003 * ANODE
      G(2660+JTEST) = G(2660+JTEST) * H1004 * ANODE
      G(2680+JTEST) = G(2080+JTEST) * H1005 * ANODE
      G(2700+JTEST) = G(2700+JTEST) * H1006 * ANODE
      G(2720+JTEST) = G(2720+JTEST) * H1007 * ANODE
      G(2740+JTEST) = G(2740+JTEST) * H1008 * ANODE
      G(2760+JTEST) = G(2760+JTEST) * H1009 * ANODE
      G(2780+JTEST) = G(2780+JTEST) * H1010 * ANODE
      G(2800+JTEST) = G(2800+JTEST) * H1011 * ANODE
      G(2820+JTEST) = G(2820+JTEST) * H1012 * ANODE
      G(2840+JTEST) = G(2840+JTEST) * H1013 * ANODE
      G(2860+JTEST) = G(2860+JTEST) * H1014 * ANODE
      G(2880+JTEST) = G(2880+JTEST) * H1015 * ANODE

 ***************************** VGA ***********************************************
      G(3200+JTEST) = G(3200+JTEST) * H1001 * ANODE
      G(3220+JTEST) = G(3220+JTEST) * H1002 * ANODE
      G(3240+JTEST) = G(3240+JTEST) * H1003 * ANODE
      G(3260+JTEST) = G(3260+JTEST) * H1004 * ANODE
      G(3280+JTEST) = G(3280+JTEST) * H1005 * ANODE
      G(3300+JTEST) = G(3300+JTEST) * H1006 * ANODE
      G(3320+JTEST) = G(3320+JTEST) * H1007 * ANODE
      G(3340+JTEST) = G(3340+JTEST) * H1008 * ANODE
      G(3360+JTEST) = G(3360+JTEST) * H1009 * ANODE
      G(3380+JTEST) = G(3380+JTEST) * H1010 * ANODE
      G(3400+JTEST) = G(3400+JTEST) * H1011 * ANODE
      G(3420+JTEST) = G(3420+JTEST) * H1012 * ANODE
      G(3440+JTEST) = G(3440+JTEST) * H1013 * ANODE
      G(3460+JTEST) = G(3460+JTEST) * H1014 * ANODE
      G(3480+JTEST) = G(3480+JTEST) * H1015 * ANODE
F20   CONTINUE
C
C
HEADER OPERATIONS DATA
BUILD COTS, PCB
      CALL STDSTL
C
C
HEADER OUTPUT CALLS, PCB
      CALL TPRINT ('PCB')
C      CALL GPRINT ('PCB')
      CALL HNQCAL ('PCB')
```

```
      CALL HNQPNT ('PCB')
       CALL QMAP ('PCB', 'QDAHP', 0)

     QCPROC = Q91154+Q91155+Q91156+Q91157+Q91158+Q91170+Q91171+Q91172
    +         +Q91173
    +         +Q91174+Q91186+Q91187+Q91188+Q91189+Q91190+Q91202+Q91203
    +         +Q91204
    +         +Q91205+Q91206+Q91218+Q91219+Q91220+Q91221+Q91222

     QBPROC = Q91182+Q91183+Q91198+Q91199+Q91214+Q91215

     QEPROC = Q91019+Q91035+Q91051+Q91067+Q91083

     QGPROC = Q91089+Q91090+Q91105+Q91106

     QHPROC = Q91108+Q91109+Q91124+Q91125

     QEIO =Q92077+Q92078+Q92093+Q92094+Q92109+Q92110+Q92125+Q92126
    +      +Q92141
    +      +Q92142

     QAVGA = Q93083+Q93084+Q93085+Q93086+Q93087+Q93099+Q93100+Q93101
    +        +Q93102
    +        +Q93103+Q93115+Q93116+Q93117+Q93118+Q93119+Q93131+Q93132
    +        +Q93133
    +        +Q93134+Q93135+Q93147+Q93148+Q93149+Q93150+Q93151

     QBVGA = Q93169+Q93170+Q93171+Q93172+Q93173+Q93185+Q93186+Q93187
    +        +Q93188
    +        +Q93189


     WRITE(*,*) '************* PROCESSOR BOARD ****************'
     WRITE(*,*) 'QC= ', QCPROC
     WRITE(*,*) 'QB= ', QBPROC
     WRITE(*,*) 'QE= ', QEPROC
     WRITE(*,*) 'QG= ', QGPROC
     WRITE(*,*) 'QH= ', QHPROC
     WRITE(*,*) ' '
     WRITE(*,*) '***************** I/O BOARD ******************'
     WRITE(*,*) 'QE= ', QEIO
     WRITE(*,*) ' '
     WRITE(*,*) '******************** VGA *********************'
     WRITE(*,*) 'QA= ', QAVGA
     WRITE(*,*) 'QB= ', QBVGA
     WRITE(*,*) ' '
     WRITE(*,*) ' '
     WRITE(*,*) ' '
     QTOT = QCPROC+QBPROC+QEPROC+QGPROC+QHPROC+QEIO+QAVGA+QBVGA
     WRITE(*,*) 'TOTAL DISS =', QTOT, 'WATTS'


END OF DATA
```

NDAT417.DAT

```
THIS FILE CONTAINS THE BOUNDARY CONDITIONS (NODE DATA) FOR FORCED
CONVECTION WITH Vair = 4.17 M/SEC.

********** CPU BOARD **********
   PCB
      GEN  1001, 240, 1, 45., -1.

   CHIP NODES
      GEN  -91019, 5, 16, 47., -1.
      GEN  -91089, 2,  1, 49., -1.
      GEN  -91105, 2,  1, 49., -1.
      GEN  -91108, 2,  1, 44., -1.
      GEN  -91124, 2,  1, 44., -1.
      GEN  -91154, 5,  1, 51., -1.
      GEN  -91170, 5,  1, 51., -1.
      GEN  -91182, 2,  1, 49., -1.
      GEN  -91186, 5,  1, 51., -1.
      GEN  -91198, 2,  1, 49., -1.
      GEN  -91202, 5,  1, 51., -1.
      GEN  -91214, 2,  1, 49., -1.
      GEN  -91218, 5,  1, 51., -1.

   PC104 CONN

      GEN  91031, 14, 16, 20., -1.
      GEN  91080,  9, 16, 20., -1.


********** I/O BOARD **********
   PCB
      GEN  2001, 240, 1, 44., -1.

   CHIP NODES
      GEN  -92077, 5, 16, 41., -1.
      GEN  -92078, 5, 16, 41., -1.

   PC104 CONN

      GEN  92031, 14, 16, 20., -1.
      GEN  92080,  9, 16, 20., -1.

********** VGA BOARD **********
   PCB
      GEN  3001, 240, 1, 20., -1.

   CHIP NODES
      GEN -93083, 5, 1, 57., -1.
      GEN -93099, 5, 1, 57., -1.
      GEN -93115, 5, 1, 57., -1.
      GEN -93131, 5, 1, 57., -1.
      GEN -93147, 5, 1, 57., -1.

      GEN -93169, 5, 1, 47., -1.
      GEN -93185, 5, 1, 47., -1.

   PC104 CONN

      GEN  93031, 14, 16, 20., -1.
      GEN  93080,  9, 16, 20., -1.
```

```
********** MIDDLE BOARD **********

   THIS BOARD REPRESENT THE LOWER BOUNDARY CONDITION (MIDDLE BOARD) AND
   IS CONNECTED VIA FREE CONVECTION TO THE BOARD EXPOSED TO THE FORCED
   AIR FLOW.

      -7771, 43., 1.
      -7772, 46., 1.
      -7773, 49., 1.

********** AIR NODES **********

      FREE STREAM AIR ABOVE CPU BOARD
      -8881, 43., 1.
      -8882, 42., 1.
      -8883, 44., 1.

********** ROOM **********

      -9999, 21., 1.
       -9999, 42., 1.
```